# UE910 Hardware User Guide

1VV0301012 Rev.13 – 2019-10-31

# Applicability Table

| PRODUCT |
|---|
| UE910-EUR |
| UE910-EUD |
| UE910-NAR |
| UE910-NAD |
| UE910-GL |

 

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# Contents



 

 

# 1 Introduction

## 1.1 Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UE910 module.

## 1.2 Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our UE910 modules.

## 1.3 Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
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TS-APAC@telit.com

Alternatively, use:
http://www.telit.com/en/products/technical-support-center/contact.php
For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:
http://www.telit.com
To register for product news and announcements or for product questions contact Telit's Technical Support Center (TTSC).
Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.
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# 1.4 Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" provides an overview of the document.

Chapter3: "UE910 Module Connections" deals with the pin out configuration and layout.

Chapter 4: "Hardware Commands" How to operate on the module via hardware.

Chapter 5: "Power supply" Power supply requirements and general design rules.

Chapter 6: "GSM/WCDMA Radio" The antenna connection and board layout design are the most important parts in the full product design.

Chapter 7: "Logic Level specifications" Specific values adopted in the implementation of logic levels for this module.

Chapter 8: "USB Port" The USB port on the Telit UE910 is the core of the interface between the module and OEM hardware

Chapter 9: "SPI port" Refers to the SPI port of the Telit UE910

Chapter 10: "USB HSIC" Refers to the USB HSIC port of the Telit UE910

Chapter 11: "Serial ports" Refers to the serial ports of the Telit UE910

Chapter 12: "Audio Section overview" Refers to the audio blocks of the Base Band Chip of the UE910 Telit Modules.

Chapter 13: "General Purpose I/O" How the general purpose I/O pads can be configured.

Chapter 14: "Mounting the UE910 on the application board" Mechanical dimensions and recommendations on how to mount the module on the user's board.

Chapter 15: "Safety Recommendations" Information related to the Safety topics.

Chapter 16: "Conformity Assessment Issues" Information related to the Conformity Assessments.

 

## 1.5 Text Conventions

***Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.***

***Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.***

**Tip or Information – Provides advice and suggestions that may be useful when integrating the module.**

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

## 1.6 Related Documents

- Digital Voice Interface Application Note 80000NT10050A
- SPI Port Application Note 80000NT10053A
- SIM Holder Design Guides 80000NT10001a
- USB HSIC Port Application Note 80000NT10071A
- AT Commands Reference Guide 80378ST10091A
- Telit EVK2 User Guide 1vv0300704

 

# 1.7 Document History

| Revision | Date | Changes |
|---|---|---|
| ISSUE#0 | 2012-09-07 | Preliminary Version |
| ISSUE#1 | 2013-04-10 | Updated Chapters 5.2, 6.3, 6.4, 9, 11, 13.4, 15 |
| ISSUE#2 | 2013-04-24 | Updated Chapters 13.4, 15.2 |
| ISSUE#3 | 2013-08-02 | Updated Chapters 4, 5.1, 6.3, 12.4, 13.4, added Reel packaging chapter |
| ISSUE#4 | 2013-08-30 | Updated Chapters 3.1, 4.1, 4.2, 5.2, 7, 8.1, 10, 12.1 |
| ISSUE#5 | 2013-12-20 | Updated Chapters 1.4, 1.6, 3.1, updated schematics and flow charts; added USB HSIC; updated packaging drawing; added PCB Guidelines for FCC. |
| ISSUE#6 | 2014-08-28 | Updated Chapter 11.2 deleted note under table |
| ISSUE#7 | 2015-05-25 | Updated Chapter 14.8 Packing system (Tray) |
| ISSUE#8 | 2016-09-01 | Updated Chapter 3.1.1 LGA Pads Layout – updated pin B1 |
| ISSUE#9 | 2016-11-30 | Updated Chapter 3.1 Pin Out – updated pin B1 (deleted from Reserved pin) |
| ISSUE#10 | 2017-04-27 | Updated with UE910-GL product |
| ISSUE#11 | 2017-06-13 | Updated Chapter 3.1 Pin Out |
| ISSUE#12 | 2017-06-13 | Modified reference to 2014/53/EU Directive; Add Chapter 12.1.4 Electrical Characteristics; |
| ISSUE#13 | 2019-10-31 | Section 14.7.1: Warning comment added<br>Added Section 16.2: ANATEL Regulatory Notices |
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# 2 Overview

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UE910 module.
In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit UE910 module. For further hardware details that may not be explained in this document refer to the Telit UE910 Product Description document where all the hardware information is reported.

**NOTICE:**
(EN) The integration of the GSM/GPRS/WCDMA **UE910** cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare GSM/GPRS/WCDMA **UE910** all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des **UE910** GSM/GPRS/WCDMA Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija GSM/GPRS/WCDMA **UE910** modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo GSM/GPRS/WCDMA **UE910** debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire GSM/GPRS/WCDMA **UE910** dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי עם המוצר. **UE910**

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# 3 UE910 module connections

## 3.1 PIN-OUT

| PAD | Signal | I/O | Function | Type | COMMENT |
|---|---|---|---|---|---|
| **USB HS 2.0 COMMUNICATION PORT** | | | | | |
| **B15** | USB_D+ | I/O | USB differential Data (+) | | |
| **C15** | USB_D- | I/O | USB differential Data (-) | | |
| **A13** | VUSB | I | Power sense for the internal USB transceiver. | | |
| **Asynchronous Serial Port (USIF0) - Prog. / Data + HW Flow Control** | | | | | |
| **N15** | C103/TXD | I | Serial data input from DTE | CMOS 1.8V | |
| **M15** | C104/RXD | O | Serial data output to DTE | CMOS 1.8V | |
| **M14** | C108/DTR | I | Input for (DTR) from DTE | CMOS 1.8V | |
| **L14** | C105/RTS | I | Input for Request to send signal (RTS) from DTE | CMOS 1.8V | |
| **P15** | C106/CTS | O | Output for Clear to Send signal (CTS) to DTE | CMOS 1.8V | |
| **N14** | C109/DCD | O | Output for (DCD) to DTE | CMOS 1.8V | |
| **P14** | C107/DSR | O | Output for (DSR) to DTE | CMOS 1.8V | |
| **R14** | C125/RING | O | Output for Ring (RI) to DTE | CMOS 1.8V | |
| **Asynchronous Auxiliary Serial Port (USIF1)** | | | | | |
| **D15** | TX_AUX | O | Auxiliary UART (TX Data to DTE) | CMOS 1.8V | |
| **E15** | RX_AUX | I | Auxiliary UART (RX Data from DTE) | CMOS 1.8V | |
| **USB HSIC** | | | | | |
| **A12** | HSIC_USB_DATA | I/O | USB HSIC data signal | CMOS 1.2V | |
| **A11** | HSIC_USB_STRB | I/O | USB HSIC strobe signal | CMOS 1.2V | |
| **H15** | HSIC_SLAVE_WAKEUP | I | Slave Wake Up | CMOS 1.8V | Shared with SPI_MRDY |
| **F15** | HSIC_HOST_WAKEUP | O | Host Wake Up | CMOS 1.8V | Shared with SPI CLK |
| **K15** | HSIC_SUSPEND_REQUEST | O | Slave Suspend Request | CMOS 1.8V | Shared with GPIO08 |
| **J15** | HSIC_HOST_ACTIVE | I | Active Host Indication | CMOS 1.8V | Shared with SPI_SRDY |
| **SIM card interface** | | | | | |
| **A6** | SIMCLK | O | External SIM signal – Clock | 1.8 / 3V | |
| **A7** | SIMRST | O | External SIM signal – Reset | 1.8 / 3V | |
| **A5** | SIMIO | I/O | External SIM signal – Data I/O | 1.8 / 3V | |
| **A4** | SIMIN | I | External SIM signal – Presence (active low) | CMOS 1.8 | |
| **A3** | SIMVCC | - | External SIM signal – Power supply for the SIM | 1.8 / 3V | |
| **Analog Audio** | | | | | |
| **B2** | EAR+ | O | Analog Audio Interface (EAR+) | | Not available on UE910-xxD/UE910-GL |

 

| | | | | | |
|---|---|---|---|---|---|
| **B3** | EAR- | O | Analog Audio Interface (EAR-) | | Not available on UE910-xxD/UE910-GL |
| **B4** | MIC+ | I | Analog Audio Interface (MIC+) | | Not available on UE910-xxD/UE910-GL |
| **B5** | MIC- | I | Analog Audio Interface (MIC-) | | Not available on UE910-xxD/UE910-GL |
| **Digital Voice Interface (DVI)** | | | | | |
| **B9** | DVI_WA0 | I/O | Digital Audio Interface (WA0) | CMOS 1.8V | |
| **B6** | DVI_RX | I/O | Digital Audio Interface (RX) | CMOS 1.8V | |
| **B7** | DVI_TX | I/O | Digital Audio Interface (TX) | CMOS 1.8V | |
| **B8** | DVI_CLK | I/O | Digital Audio Interface (CLK) | CMOS 1.8V | |
| **SPI** | | | | | |
| **D15** | SPI_MOSI | I | SPI MOSI | CMOS 1.8V | Shared with TX_AUX |
| **E15** | SPI_MISO | O | SPI_MISO | CMOS 1.8V | Shared with RX_AUX |
| **F15** | SPI_CLK | I | SPI Clock | CMOS 1.8V | |
| **H15** | SPI_MRDY | I | SPI_MRDY | CMOS 1.8V | |
| **J15** | SPI_SRDY | O | SPI_SRDY | CMOS 1.8V | |
| **DIGITAL IO** | | | | | |
| **C8** | GPIO_01 | I/O | GPIO_01 /STAT LED | CMOS 1.8V | Alternate Function STAT LED |
| **C9** | GPIO_02 | I/O | GPIO_02 | CMOS 1.8V | |
| **C10** | GPIO_03 | I/O | GPIO_03 | CMOS 1.8V | |
| **C11** | GPIO_04 | I/O | GPIO_04 | CMOS 1.8V | |
| **B14** | GPIO_05 | I/O | GPIO_05 | CMOS 1.8V | |
| **C12** | GPIO_06 | I/O | GPIO_06 | CMOS 1.8V | |
| **C13** | GPIO_07 | I/O | GPIO_07 | CMOS 1.8V | |
| **K15** | GPIO_08 | I/O | GPIO_08 | CMOS 1.8V | |
| **L15** | GPIO_09 | I/O | GPIO_09 | CMOS 1.8V | |
| **G15** | GPIO_10 | I/O | GPIO_10 | CMOS 1.8V | |
| **ADC** | | | | | |
| **B1** | ADC_IN1 | AI | Analog / Digital converter input | A/D | Accepted values 0 to 1.2V DC |
| **RF SECTION** | | | | | |
| **K1** | ANTENNA | I/O | GSM/EDGE/UMTS Antenna (50 ohm) | RF | |
| **Miscellaneous Functions** | | | | | |
| **R13** | HW_SHUTDOWN* | I | HW Unconditional Shutdown | CMOS 1.8V | Active low |
| **R12** | ON_OFF* | I | Input command for power ON | CMOS 1.8V | Active low |
| **C14** | VRTC | I | VRTC Backup capacitor | Power | backup for the embedded RTC supply |
| **R11** | VAUX/PWRMON | O | Supply Output for external accessories / Power ON Monitor | 1.8V | |
| **Power Supply** | | | | | |
| **M1** | VBATT | - | Main power supply (Baseband) | Power | |
| **M2** | VBATT | - | Main power supply (Baseband) | Power | |
| **N1** | VBATT_PA | - | Main power supply (Radio PA) | Power | |

 

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|---|---|---|---|---|---|
| **N2** | VBATT_PA | - | Main power supply (Radio PA) | Power | |
| **P1** | VBATT_PA | - | Main power supply (Radio PA) | Power | |
| **P2** | VBATT_PA | - | Main power supply (Radio PA) | Power | |
| **E1** | GND | - | Ground | Power | |
| **G1** | GND | - | Ground | Power | |
| **H1** | GND | - | Ground | Power | |
| **J1** | GND | - | Ground | Power | |
| **L1** | GND | - | Ground | Power | |
| **A2** | GND | - | Ground | Power | |
| **E2** | GND | - | Ground | Power | |
| **F2** | GND | - | Ground | Power | |
| **G2** | GND | - | Ground | Power | |
| **H2** | GND | - | Ground | Power | |
| **J2** | GND | - | Ground | Power | |
| **K2** | GND | - | Ground | Power | |
| **L2** | GND | - | Ground | Power | |
| **R2** | GND | - | Ground | Power | |
| **M3** | GND | - | Ground | Power | |
| **N3** | GND | - | Ground | Power | |
| **P3** | GND | - | Ground | Power | |
| **R3** | GND | - | Ground | Power | |
| **D4** | GND | - | Ground | Power | |
| **M4** | GND | - | Ground | Power | |
| **N4** | GND | - | Ground | Power | |
| **P4** | GND | - | Ground | Power | |
| **R4** | GND | - | Ground | Power | |
| **N5** | GND | - | Ground | Power | |
| **P5** | GND | - | Ground | Power | |
| **R5** | GND | - | Ground | Power | |
| **N6** | GND | - | Ground | Power | |
| **P6** | GND | - | Ground | Power | |
| **R6** | GND | - | Ground | Power | |
| **P8** | GND | - | Ground | Power | |
| **R8** | GND | - | Ground | Power | |
| **P9** | GND | - | Ground | Power | |
| **P10** | GND | - | Ground | Power | |
| **R10** | GND | - | Ground | Power | |
| **M12** | GND | - | Ground | Power | |
| **B13** | GND | - | Ground | Power | |
| **P13** | GND | - | Ground | Power | |
| **E14** | GND | - | Ground | Power | |

 

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|---|---|---|---|---|---|
| **RESERVED** | | | | | |
| **C1** | RESERVED | - | RESERVED | | |
| **D1** | RESERVED | - | RESERVED | | |
| **B2** | RESERVED | - | RESERVED | | |
| **C2** | RESERVED | - | RESERVED | | |
| **D2** | RESERVED | - | RESERVED | | |
| **B3** | RESERVED | - | RESERVED | | |
| **C3** | RESERVED | - | RESERVED | | |
| **D3** | RESERVED | - | RESERVED | | |
| **E3** | RESERVED | - | RESERVED | | |
| **F3** | RESERVED | - | RESERVED | | |
| **G3** | RESERVED | - | RESERVED | | |
| **H3** | RESERVED | - | RESERVED | | |
| **J3** | RESERVED | - | RESERVED | | |
| **K3** | RESERVED | - | RESERVED | | |
| **L3** | RESERVED | - | RESERVED | | |
| **B4** | RESERVED | - | RESERVED | | |
| **C4** | RESERVED | - | RESERVED | | |
| **B5** | RESERVED | - | RESERVED | | |
| **C5** | RESERVED | - | RESERVED | | |
| **C6** | RESERVED | - | RESERVED | | |
| **C7** | RESERVED | - | RESERVED | | |
| **N7** | RESERVED | - | RESERVED | | |
| **P7** | RESERVED | - | RESERVED | | |
| **N8** | RESERVED | - | RESERVED | | |
| **N9** | RESERVED | - | RESERVED | | |
| **A10** | RESERVED | - | RESERVED | | |
| **N10** | RESERVED | - | RESERVED | | |
| **N11** | RESERVED | - | RESERVED | | |
| **B12** | RESERVED | - | RESERVED | | |
| **D12** | RESERVED | - | RESERVED | | |
| **N12** | RESERVED | - | RESERVED | | |
| **P12** | RESERVED | - | RESERVED | | |
| **F14** | RESERVED | - | RESERVED | | |
| **G14** | RESERVED | - | RESERVED | | |
| **H14** | RESERVED | - | RESERVED | | |
| **J14** | RESERVED | - | RESERVED | | |
| **K14** | RESERVED | - | RESERVED | | |
| **N13** | RESERVED | - | RESERVED | | |
| **L13** | RESERVED | - | RESERVED | | |
| **J13** | RESERVED | - | RESERVED | | |
| **M13** | RESERVED | - | RESERVED | | |

 

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|---|---|---|---|---|---|
| **K13** | RESERVED | - | RESERVED | | |
| **H13** | RESERVED | - | RESERVED | | |
| **G13** | RESERVED | - | RESERVED | | |
| **F13** | RESERVED | - | RESERVED | | |
| **B11** | RESERVED | - | RESERVED | | |
| **B10** | RESERVED | - | RESERVED | | |
| **A9** | RESERVED | - | RESERVED | | |
| **A8** | RESERVED | - | RESERVED | | |
| **D14** | RESERVED | - | RESERVED | | |
| **A14** | RESERVED | - | RESERVED | | |
| **D13** | RESERVED | - | RESERVED | | |
| **E13** | RESERVED | - | RESERVED | | |
| **F1** | RESERVED | - | RESERVED | | |
| **R9** | RESERVED | - | RESERVED | | |
| **R7** | RESERVED | - | RESERVED | | |
| **P11** | RESERVED | - | RESERVED | | |

**WARNING:**

Reserved pins must not be connected.

**NOTE 1:**
The following table is listing the main Pinout differences between the UE910 variants

| Product | Audio | Notes |
|---|---|---|
| UE910-EUR | YES | Analog and digital audio |
| UE910-EUD | NO | Reserved Pads:,B2, B3, B4, B5 |
| UE910-NAR | YES | Analog and digital audio |
| UE910-NAD | NO | Reserved Pads:,B2, B3, B4, B5 |
| UE910-GL | YES | Digital Audio; Reserved Pads:B2, B3, B4, B5 |

NOTE:

If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

| PAD | Signal | Notes |
|---|---|---|
| M1,M2,N1,N2,P1,P2 | VBATT & VBATT_PA | |
| E1,G1,H1,J1,L1,A2,E2,F2,G2,H2, J2,K2,L2,R2,M3,N3,P3,R3,D4,M4, N4,P4,R4,N5,P5,R5,N6,P6,R6,P8, R8,P9,P10,R10,M12,B13,P13,E14 | GND | |
| R12 | ON/OFF* | |
| R13 | HW_SHUTDOWN* | |
| B15 | USB_D+ | If not used should be connected to a Test Point or an USB connector |
| C15 | USB_D- | If not used should be connected to a Test Point or an USB connector |
| A13 | VUSB | If not used should be connected to a Test Point or an USB connector |
| N15 | C103/TXD | If not used should be connected to a Test Point |
| M15 | C104/RXD | If not used should be connected to a Test Point |
| L14 | C105/RTS | If the flow control is not used it should be connected to GND |
| P15 | C106/CTS | If not used should be connected to a Test Point |
| D15 | TXD_AUX | If not used should be connected to a Test Point |
| E15 | RXD_AUX | If not used should be connected to a Test Point |
| K1 | MAIN ANTENNA | |

RTS pin should be connected to the GND (on the module side) if flow control is not used.

The above pins are also necessary to debug the application when the module is assembled on it so we recommend connecting them also to dedicated test point.

## 3.1.1 LGA Pads Layout

TOP VIEW

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | ADC_IN1 | RES | RES | GND | RES | GND | GND | GND | ANT | GND | VBATT | VBATT_PA | VBATT_PA | |
| 2 | GND | SPK+ | RES | RES | GND | GND | GND | GND | GND | GND | GND | VBATT | VBATT_PA | VBATT_PA | GND |
| 3 | SIMVCC | SPK - | RES | RES | RES | RES | RES | RES | RES | RES | RES | GND | GND | GND | GND |
| 4 | SIMIN | MIC+ | RES | GND | | | | | | | | GND | GND | GND | GND |
| 5 | SIMIO | MIC - | RES | | | | | | | | | | GND | GND | GND |
| 6 | SIMCLK | DVI_RX | RES | | | | | | | | | | GND | GND | GND |
| 7 | SIMRST | DVI_TX | RES | | | | | | | | | | RES | RES | RES |
| 8 | RES | DVI_CLK | GPIO_01 | | | | | | | | | | RES | GND | GND |
| 9 | RES | DVI_WA0 | GPIO_02 | | | | | | | | | | RES | GND | RES |
| 10 | RES | RES | GPIO_03 | | | | | | | | | | RES | GND | GND |
| 11 | HSIC_USB_STRB | RES | GPIO_04 | | | | | | | | | | RES | RES | VAUX/PWRMON |
| 12 | HSIC_USB_DATA | RES | GPIO_06 | RES | | | | | | | | GND | RES | RES | ON_OFF* |
| 13 | VUSB | GND | GPIO_07 | RES | RES | RES | RES | RES | RES | RES | RES | RES | RES | GND | HW_SHUTDOWN* |
| 14 | RES | GPIO_05 | VRTC | RES | GND | RES | RES | RES | RES | RES | C105/RTS | C108/DTR | C109/DCD | C107/DSR | C125/RING |
| 15 | | USB_D+ | USB_D- | TX AUX | RX AUX | SPI_CLK | GPIO_10 | SPI_MRDY | SPI_SRDY | GPIO_08 | GPIO_09 | C104/RXD | C103/TXD | C106/CTS | |

**NOTE:**

The pin defined as **RES** has to be considered RESERVED and not connected on any pin in the application.

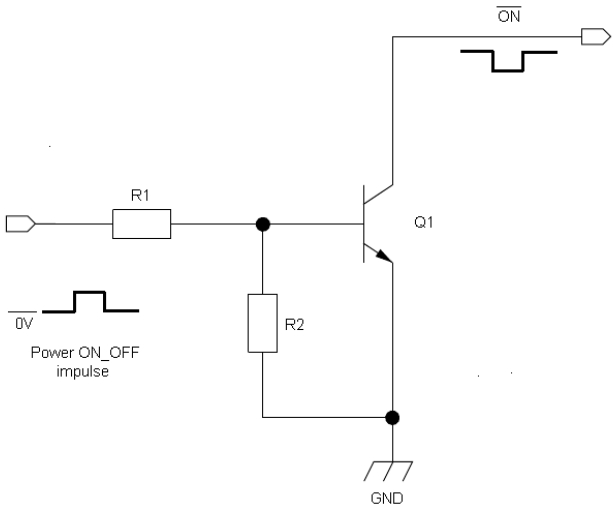
 

# 4 Hardware Commands

## 4.1 Turning ON the UE910

To turn on the UE910 the pad ON_OFF* must be tied low for at least 5 seconds and then released.

The maximum current that can be drained from the ON_OFF* pad is 0,1 mA.
A simple circuit to do it is:




**NOTE:**

Don't use any pull up resistor on the ON_OFF* line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the UE910 power regulator and improper power on/off of the module. The line ON_OFF* must be connected only in open collector or open drain configuration.

**NOTE:**

In this document all the lines that are inverted, hence have active low signals are labelled with a name that ends with"#","*" or with a bar over the name.

**TIP:**

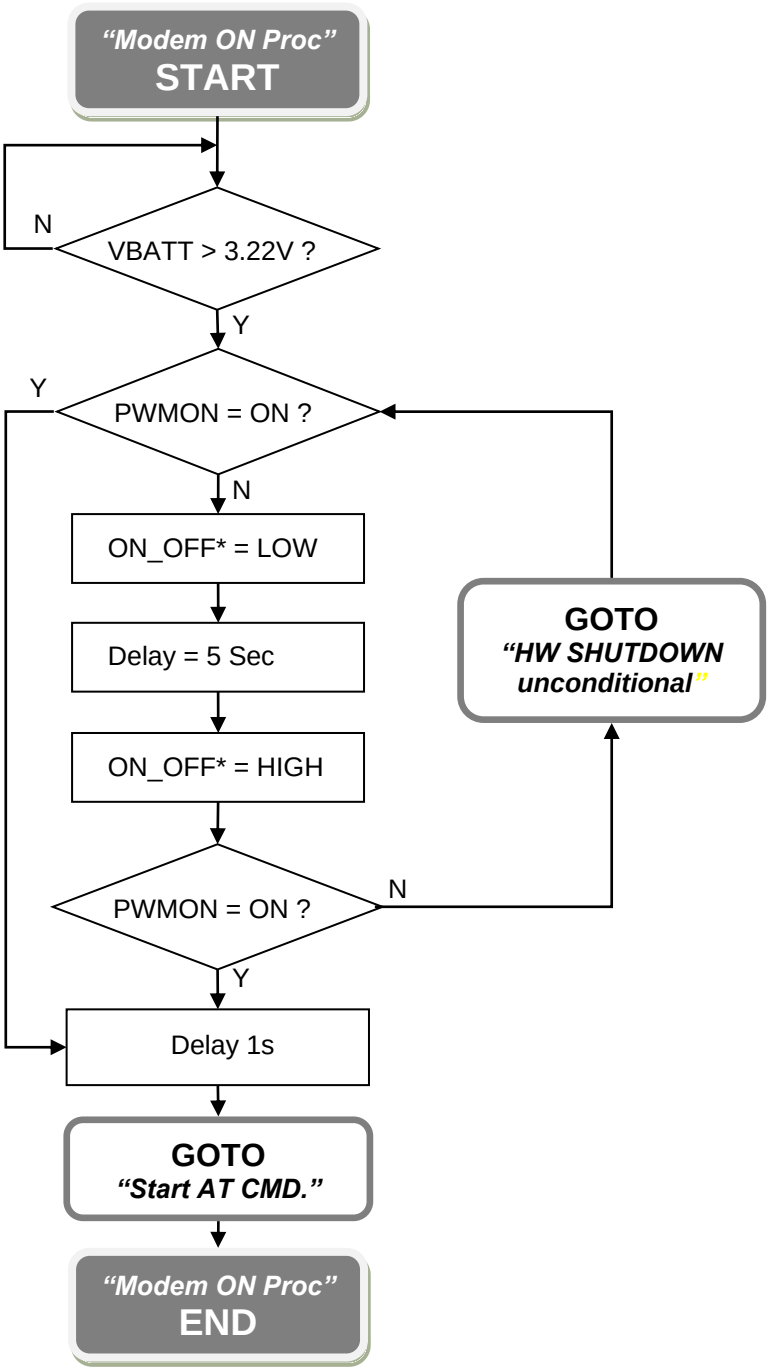
To check if the device has powered on, the hardware line PWRMON should be monitored.

**NOTE:**

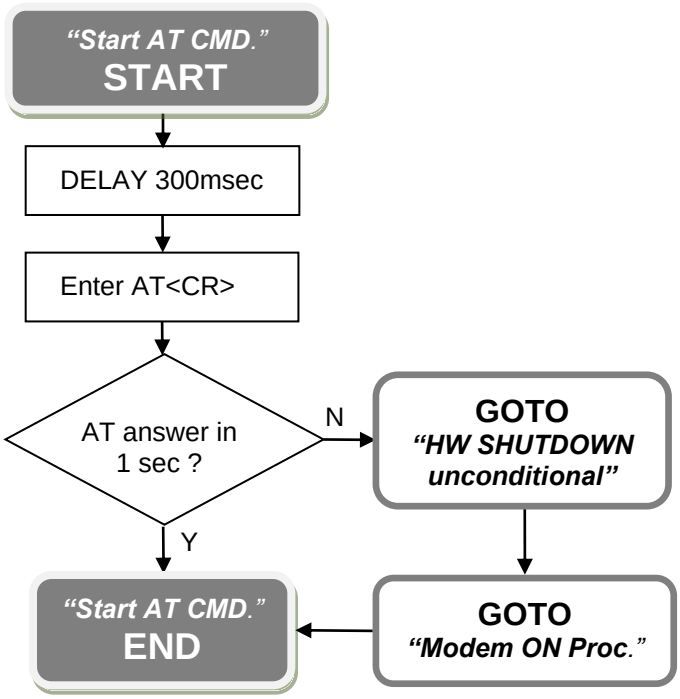
It is mandatory to avoid sending data to the serial ports during the first 200ms of the module start-up.

A flow chart showing the proper turn on procedure is displayed below:



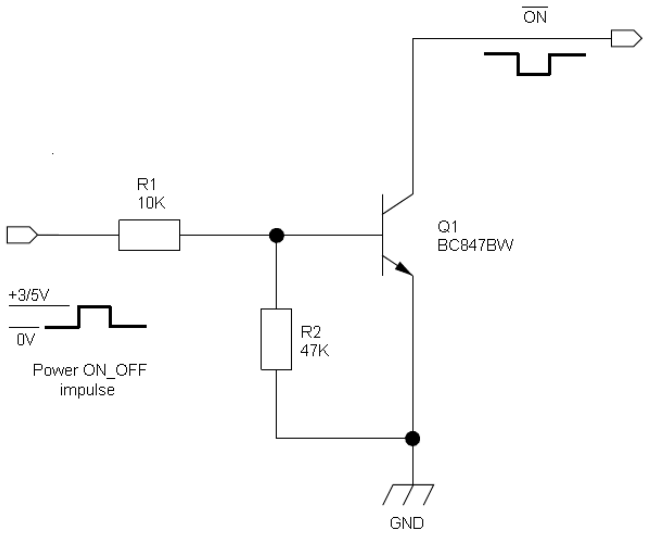
A flow chart showing the AT commands managing procedure is displayed below:



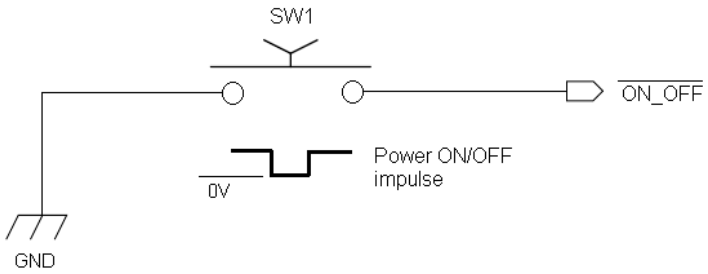
**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

For example:
1- Let's assume you need to drive the ON_OFF* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT1):



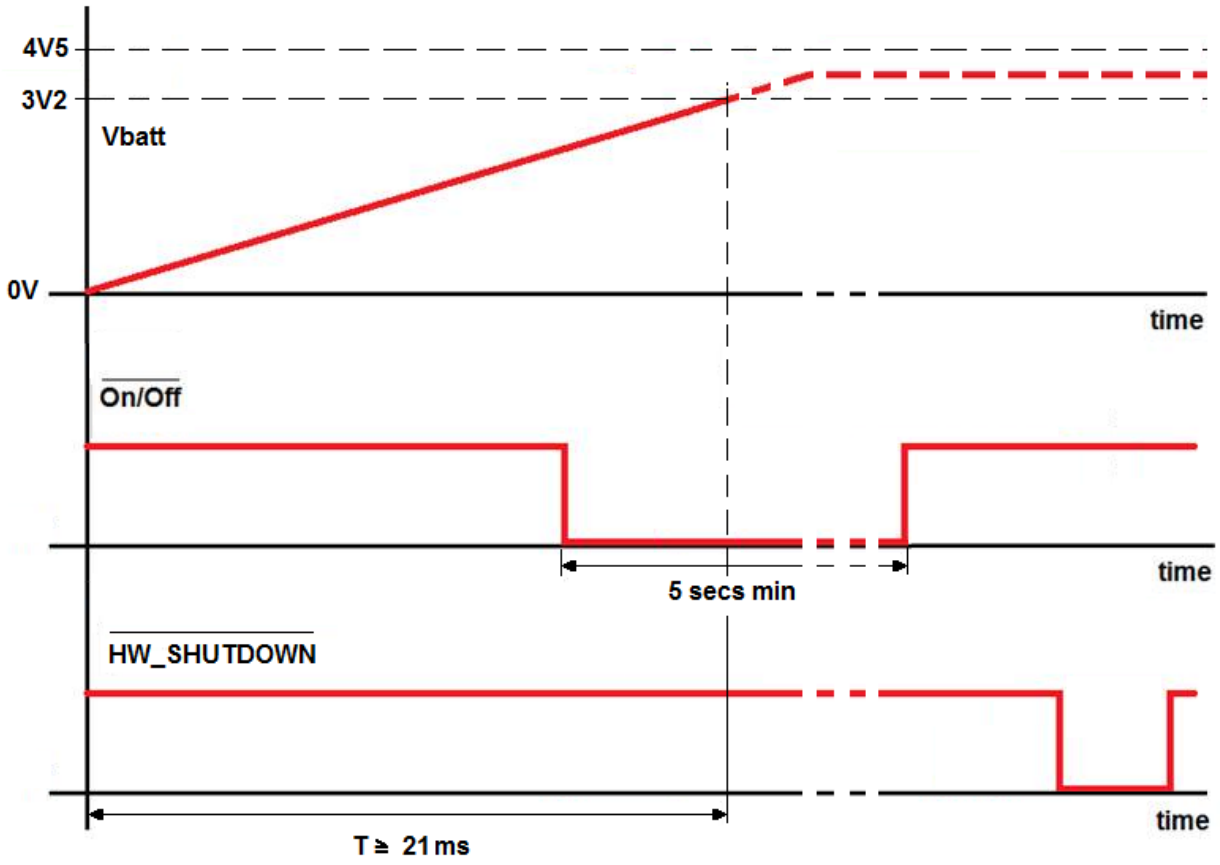

2- Let's assume you need to drive the ON_OFF* pad directly with an ON/OFF button:




**WARNING**
It is recommended to set the ON_OFF* line LOW to power on the module only after VBATT is higher than 3.22V.
In case this condition it is not satisfied you could use the HW_SHUTDOWN* line to recover it and then restart the power on activity using the ON_OFF * line.

An example of this is described in the following diagram:




After HW_SHUTSDOWN* is released you could again use the ON_OFF* line to power on the module.

# 4.2 Turning OFF the UE910

Turning off of the device can be done in two ways:

- via AT command (see UE910 Software User Guide, AT#SHDN)
- by tying low pin ON_OFF*

Either ways, the device issues a detach request to network informing that the device will not be reachable any more.
To turn OFF the UE910 the pad ON_OFF* must be tied low for at least 3 seconds and then released.

**TIP:**

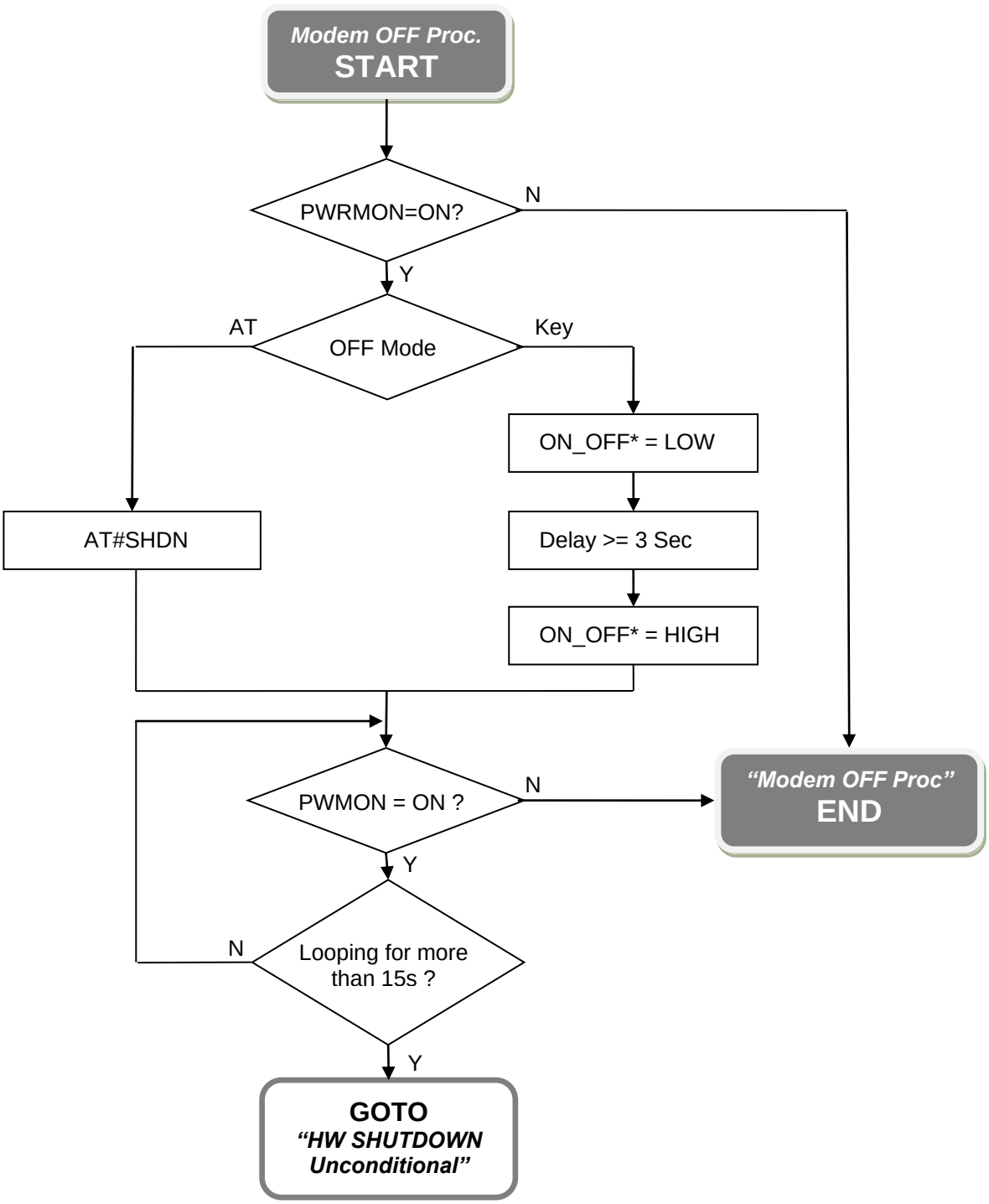
To check if the device has been powered off, the hardware line PWRMON must be monitored. The device is powered off when PWRMON goes low.

**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

The following flow chart shows the proper turn off procedure:



# 4.3 UE910 Unconditional Shutdown

The Unconditional Shutdown of the module could be activated using the HW_SHUTDOWN* line (pad R13).

**WARNING:**

The hardware unconditional Shutdown must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure.

To unconditionally shutdown the UE910, the pad HW_SHUTDOWN* must be tied low for at least 200 milliseconds and then released.

**NOTE:**

Do not use any pull up resistor on the HW_SHUTDOWN* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the UE910 power regulator and improper functioning of the module. The line HW_SHUTDOWN* must be connected only in open collector configuration.

The HW_SHUTDOWN* is generating an unconditional shutdown of the module without an automatic restart.

The module will shutdown, but will NOT perform the detach from the cellular network.

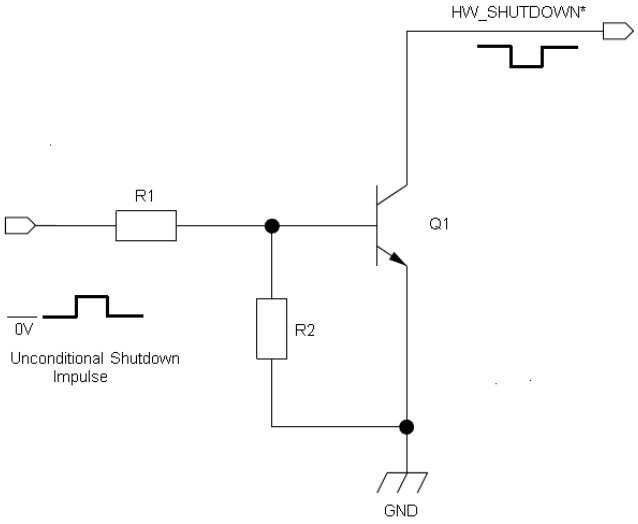
To proper power on again the module please refer to the related paragraph (“Powering ON the UE910”)

**TIP:**

The unconditional hardware shutdown must always be implemented on the boards and should be used only as an emergency exit procedure.

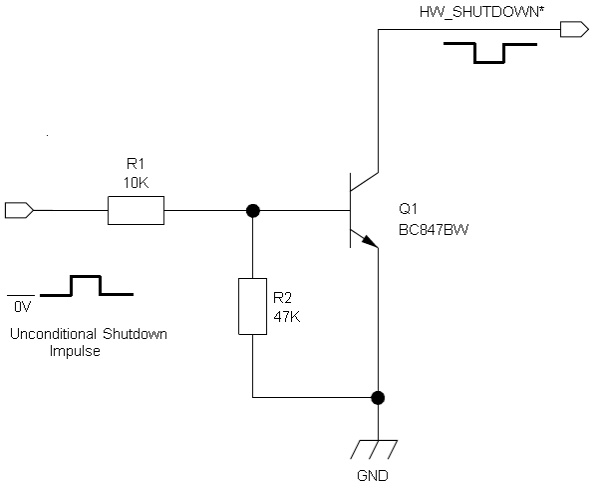
 

A typical circuit is the following:




For example:

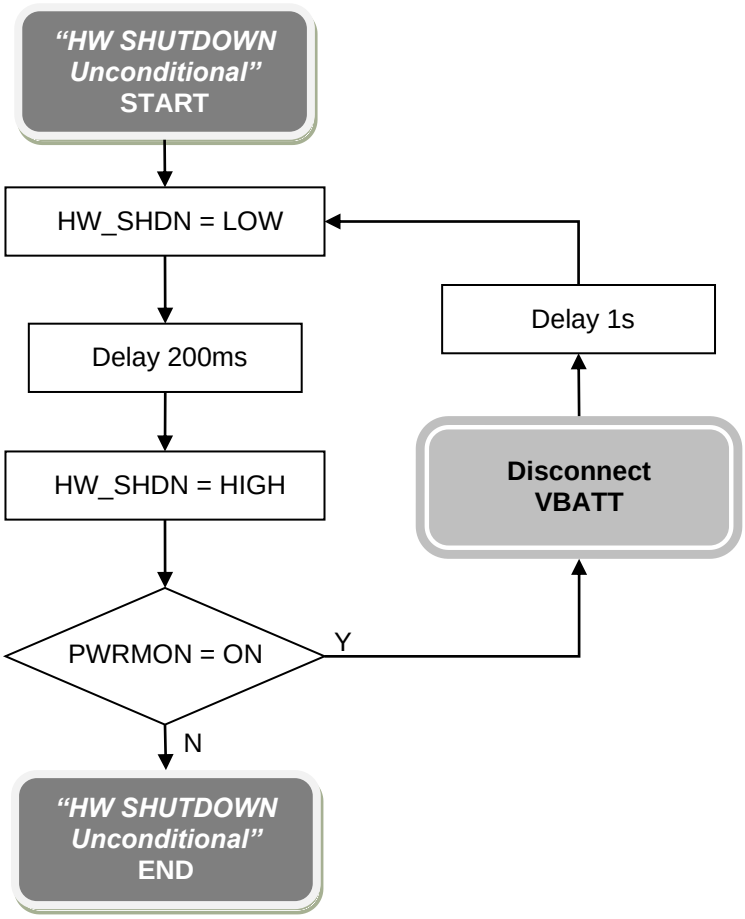
1- Let us assume you need to drive the HW_SHUTDOWN* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT2):




**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

In the following flow chart is detailed the proper restart procedure:



# 5 Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

## 5.1 Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfil the following requirements:

| POWER SUPPLY | |
|---|---|
| Nominal Supply Voltage | 3.8 V |
| Normal Operating Voltage Range | 3.40 V÷ 4.20 V |
| Extended Operating Voltage Range | 3.10 V÷ 4.50 V |

**NOTE:**

The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

The Power supply must be higher than 3.22 V to power on the module

**NOTE:**

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;

The "Extended Operating Voltage Range" can be used only with completely assumption and application of the HW User guide suggestions.

# 5.2 Power Consumption

| UE910 | | |
|---|---|---|
| **Mode** | **Average (mA)** | **Mode description** |
| **SWITCHED OFF** | | Module supplied but Switched Off |
| Switched Off | 180 uA | |
| **IDLE mode (WCDMA)** | | |
| AT+CFUN=1 | 12.2 | Normal mode: full functionality of the module |
| AT+CFUN=5 | 1.8 | Full functionality with power saving; DRX7;<br>Module registered on the network can receive incoming calls and SMS |
| **IDLE mode (GSM/EDGE)** | | |
| AT+CFUN=1 | 19 | Normal mode: full functionality of the module |
| AT+CFUN=4 | 16.5 | Module is not registered on the network |
| AT+CFUN=5 | 1.2 | Full functionality with power saving;<br>DRX9 (1.3mA in case of DRX5). |
| **Operative mode (WCDMA)** | | |
| WCDMA Voice | 152 | WCDMA voice call (TX = 10dBm) |
| WCDMA HSDPA (0dBm) | 187 | WCDMA data call (Cat 8, TX = 0dBm) |
| WCDMA HSDPA (22dBm) | 494 | WCDMA data call (Cat 8, TX = 22dBm) |
| **Operative mode (EDGE)** | | |
| **EDGE 4TX+1RX** | | EDGE Sending data mode |
| GSM 850/900 - G8 | 495 | |
| DCS1800/ PCS1900 – G7 | 484 | |
| **Operative mode (GSM)** | | |
| **CSD TX and RX mode** | | GSM VOICE CALL |
| GSM 850/900 CSD PL5 | 220 | |
| DCS1800/ PCS1900 CSD PL0 | 167 | |
| **GPRS 4TX+1RX** | | GPRS Sending data mode |
| GSM 850/900 PL5 | 580 | |
| DCS1800/ PCS1900 PL0 | 438 | |

The GSM system is made in a way that the RF transmission is not continuous, else it is packed into bursts at a base frequency of about 216 Hz, and the relative current peaks can be as high as about 2A. Therefore the power supply has to be designed in order to withstand with these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow. If the layout of the PCB is not well designed a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible annoying noise at 216 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.

**NOTE:**

The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2 A.

The UE910-EUx variants are supporting EDGE class 33; the NAx variants support EDGE class 10.

# 5.3 General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

## 5.3.1 Electrical Design Guidelines

The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

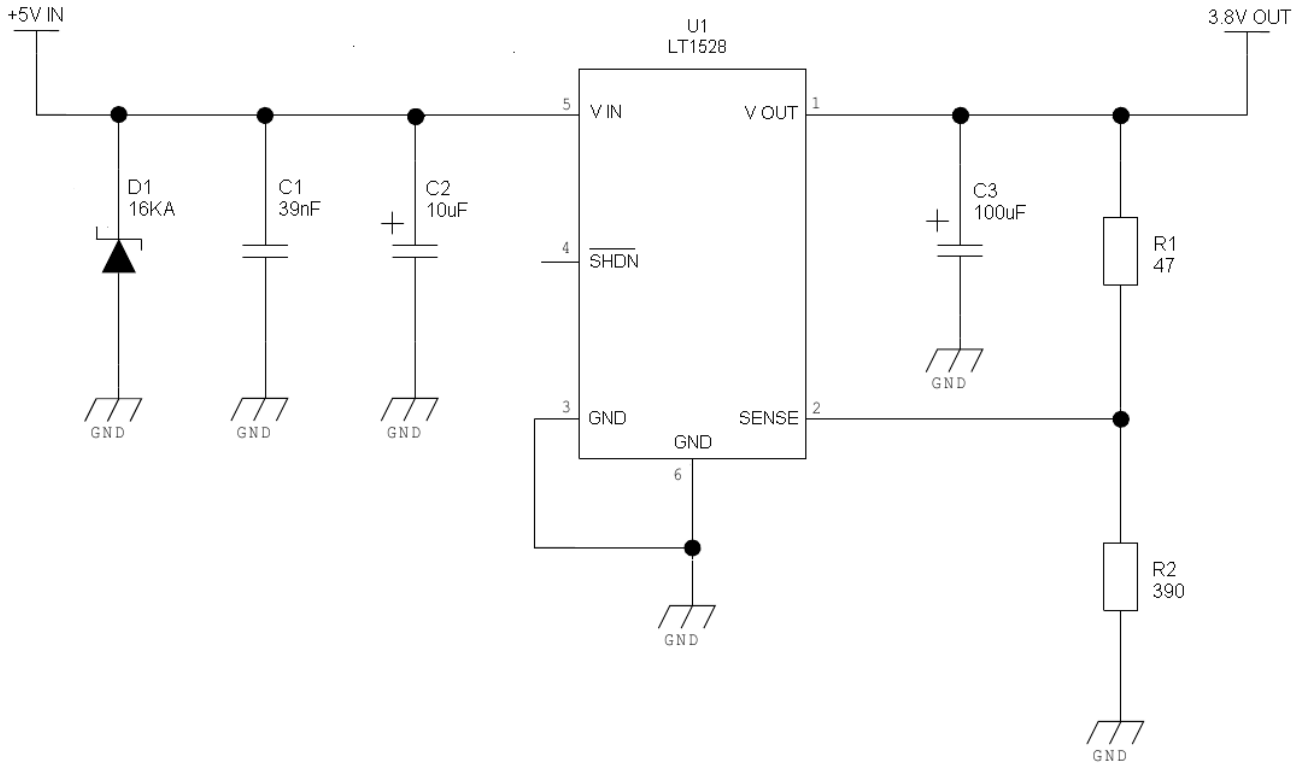
- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

### 5.3.1.1 + 5V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the UE910, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the UE910 from power polarity inversion.

An example of linear regulator with 5V input is:



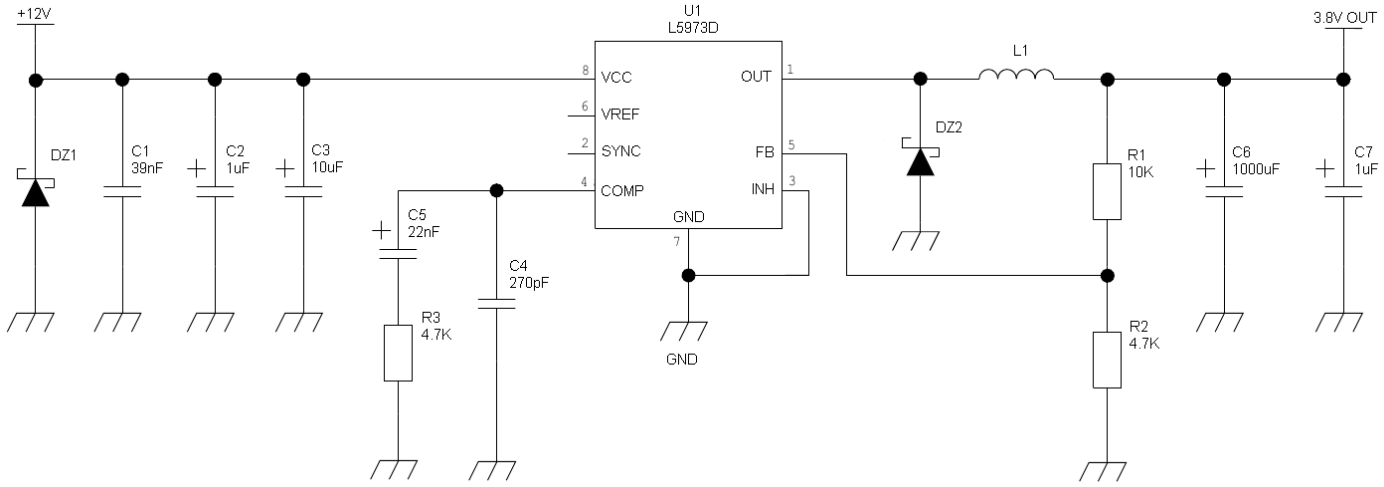

### 5.3.1.2 + 12V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by the UE910.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.

- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the UE910 from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic:



#### 5.3.1.3 Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit UE910 module.

**WARNING:**

The three cells Ni/Cd or Ni/MH 3,6 V Nom. battery types or 4V PB types ***MUST NOT BE USED DIRECTLY*** since their maximum voltage can rise over the absolute maximum voltage for the UE910 and damage it.

**NOTE:**

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with UE910. Their use can lead to overvoltage on the UE910 and damage it. USE ONLY Li-Ion battery types.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the UE910 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

## 5.3.2 Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- Average current consumption during HSDPA transmission @PWR level max :

  600 mA

- *Average current during idle:*
  1.5 *mA*

**NOTE:**

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.
If we assume that the device stays into transmission for short periods of time (let's say few minutes) and then remains for a quite long time in idle (let's say one hour), then the power supply has always the time to cool down between the calls and the heat sink could be smaller than the calculated one for 600mA maximum RMS current, or even could be the simple chip package (no heat sink).
Moreover in the average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than the 600mA, being usually around 150mA.
For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.
For the heat generated by the UE910, you can consider it to be during transmission 1W max during CSD/VOICE calls and 2W max during class12 GPRS upload.
This generated heat will be mostly conducted to the ground plane under the UE910; you must ensure that your application can dissipate it.

### 5.3.3 Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit UE910 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the UE910 is wide enough to ensure a dropless connection even during the 2A current peaks.

- The protection diode must be placed close to the input connector where the power source is drained.

- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application doesn't have audio interface but only uses the data feature of the Telit UE910, then this noise is not so disturbing and power supply layout design can be more forgiving.

- The PCB traces to the UE910 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.

- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).

- The use of a good common ground plane is suggested.

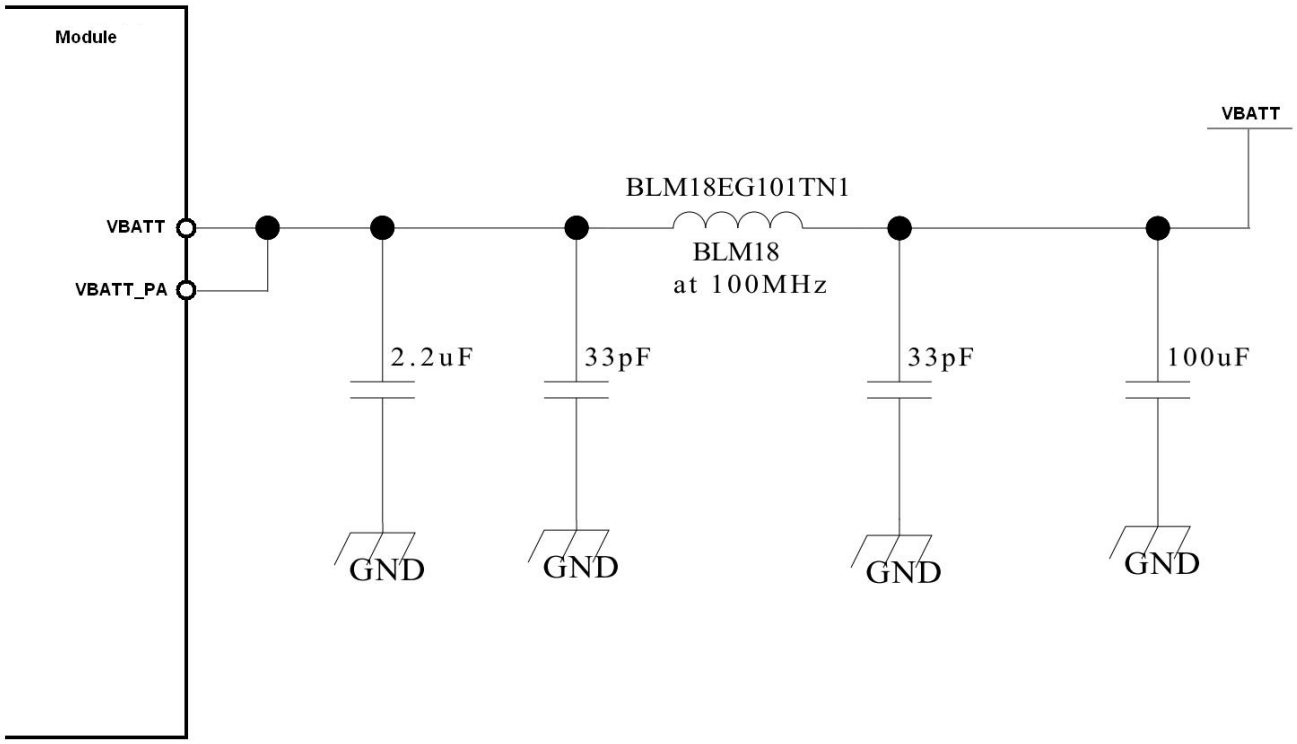
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.

- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.

- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.
  A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

  The below figure shows the recommended circuit:



# 6 GSM/WCDMA Radio Section

## 6.1 UE910 Product Variants

The following table is listing the main differences between the UE910 variants:

| Product | Supported 2G Bands | Supported 3G bands |
|---|---|---|
| **UE910-EUR** | GSM 900, DCS1800 | FDD B1, B8 |
| **UE910-EUD** | GSM 900, DCS1800 | FDD B1, B8 |
| **UE910-NAR** | GSM 850, PCS 1900 | FDD B2, B5 |
| **UE910-NAD** | GSM 850, PCS 1900 | FDD B2, B5 |
| **UE910-GL** | GSM 850, GSM 900, DCS 1800, PCS 1900 | FDD B1, B2, B5, B8 |

## 6.2 TX Output Power

**UE910-EUR & UE910-EUD**

| Band | Power Class |
|---|---|
| **GSM 900** | 4 (2W) |
| **DCS 1800** | 1 (1W) |
| **EDGE, 900 MHz** | E2 (0.5W) |
| **EDGE, 1800 MHz** | Class E2 (0.4W) |
| **WCDMA FDD B1, B8** | Class 3 (0.25W) |

**UE910-NAR & UE910-NAD**

| Band | Power Class |
|---|---|
| **GSM 850** | 4 (2W) |
| **PCS 1900** | 1 (1W) |
| **EDGE, 850 MHz** | E2 (0.5W) |
| **EDGE, 1900 MHz** | Class E2 (0.4W) |
| **WCDMA FDD B2, B5** | Class 3 (0.25W) |

## Sensitivity

**UE910-GL**

| Band | Power Class |
|---|---|
| **GSM 850, GSM 900** | 4 (2W) |
| **DCS 1800, PCS 1900** | 1 (1W) |
| **EDGE, 850/900 MHz** | E2 (0.5W) |
| **EDGE, 1800/1900 MHz** | Class E2 (0.4W) |
| **WCDMA FDD B1, B2, B5, B8** | Class 3 (0.25W) |

**UE910-EUR and UE910-EUD**

| Band | Typical | Note |
|---|---|---|
| **GSM 900** | -109 dBm | BER Class II <2.44% |
| **DCS1800** | -110 dBm | BER Class II <2.44% |
| **WCDMA FDD B1** | -111 dBm | BER <0.1% |
| **WCDMA FDD B8** | -110 dBm | BER <0.1% |

**UE910-NAR and UE910-NAD**

| Band | Typical | Note |
|---|---|---|
| **GSM 850** | -109.5 dBm | BER Class II <2.44% |
| **PCS 1900** | -109.5 dBm | BER Class II <2.44% |
| **WCDMA FDD B2** | -110 dBm | BER <0.1% |
| **WCDMA FDD B5** | -111 dBm | BER <0.1% |

**UE910-GL**

| Band | Typical | Note |
|---|---|---|
| **GSM 900** | -109 dBm | BER Class II <2.44% |
| **GSM 850** | -109.5 dBm | BER Class II <2.44% |
| **DCS1800** | -110 dBm | BER Class II <2.44% |
| **PCS 1900** | -109.5 dBm | BER Class II <2.44% |
| **WCDMA FDD B1** | -111 dBm | BER <0.1% |
| **WCDMA FDD B2** | -110 dBm | BER <0.1% |
| **WCDMA FDD B5** | -111 dBm | BER <0.1% |
| **WCDMA FDD B8** | -110 dBm | BER <0.1% |

## 6.3 GSM/WCDMA Antenna Requirements

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.
The antenna and antenna transmission line on PCB for a Telit UE910 device shall fulfil the following requirements:

| ANTENNA REQUIREMENTS (UE910-EUR and UE910-EUD) | |
|---|---|
| **Frequency range** | Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s) |
| **Bandwidth (GSM/EDGE)** | 80 MHz in GSM900<br>170 MHz in DCS |
| **Bandwidth (WCDMA)** | 250 MHz in WCDMA Band I<br>80 MHz in WCDMA Band VIII |
| **Impedance** | 50 ohm |
| **Input power** | > 33dBm(2 W) peak power in GSM<br>> 24dBm Average power in WCDMA |
| **VSWR absolute max** | ≤ 10:1 (limit to avoid permanent damage) |
| **VSWR recommended** | ≤ 2:1 (limit to fulfil all regulatory requirements) |

| ANTENNA REQUIREMENTS (UE910-NAR and UE910-NAD) | |
|---|---|
| **Frequency range** | Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s) |
| **Bandwidth (GSM/EDGE)** | 70 MHz in GSM850<br>140 MHz PCS 1900 band |
| **Bandwidth (WCDMA)** | 140 MHz in WCDMA Band II<br>70 MHz in WCDMA Band V |
| **Impedance** | 50 ohm |
| **Input power** | > 33dBm(2 W) peak power in GSM<br>> 24dBm Average power in WCDMA |

| | |
|---|---|
| **VSWR absolute max** | ≤ 10:1 (limit to avoid permanent damage) |
| **VSWR recommended** | ≤ 2:1 (limit to fulfil all regulatory requirements) |

| **ANTENNA REQUIREMENTS (UE910-GL)** | |
|---|---|
| **Frequency range** | Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s) |
| **Bandwidth (GSM/EDGE)** | 80 MHz in GSM900<br>70 MHz in GSM850<br>170 MHz in DCS 1800<br>140 MHz PCS 1900 band |
| **Bandwidth (WCDMA)** | 250 MHz in WCDMA Band I<br>140 MHz in WCDMA Band II<br>70 MHz in WCDMA Band V<br>80 MHz in WCDMA Band VIII |
| **Impedance** | 50 ohm |
| **Input power** | > 33dBm(2 W) peak power in GSM<br>> 24dBm Average power in WCDMA |
| **VSWR absolute max** | ≤ 10:1 (limit to avoid permanent damage) |
| **VSWR recommended** | ≤ 2:1 (limit to fulfil all regulatory requirements) |

When using the UE910, since there's no antenna connector on the module, the antenna must be connected to the UE910 antenna pad (K1) by means of a transmission line implemented on the PCB.

In the case the antenna is not directly connected at the antenna pad of the UE910, then a PCB line is needed in order to connect with it or with its connector.

This transmission line shall fulfil the following requirements:

| **ANTENNA LINE ON PCB REQUIREMENTS** | |
|---|---|
| Characteristic Impedance | 50 ohm |
| Max Attenuation | 0,3 dB |
| Coupling with other signals shall be avoided | |
| Cold End (Ground Plane) of antenna shall be equipotential to the UE910 ground pins | |

Furthermore if the device is developed for the US market and/or Canada market, it shall comply with the FCC and/or IC approval requirements:
This device is to be used only for mobile and fixed application. In order to re-use the Telit FCC/IC approvals the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. If antenna is installed with a separation distance of less than 20 cm from all persons or is co-located or operating in conjunction with any other antenna or transmitter then additional FCC/IC testing may be required. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance.

Antennas used for this OEM module must not exceed the gains for mobile and fixed operating configurations as described in “FCC/IC Regulatory notices” chapter.

## 6.4 GSM/WCDMA - PCB line Guidelines

- Make sure that the transmission line’s characteristic impedance is 50ohm ;
- Keep line on the PCB as short as possible, since the antenna line loss shall be less than around 0,3 dB;
- Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves;
- Any kind of suitable geometry / structure (Microstrip, Stripline, Coplanar, Grounded Coplanar Waveguide...) can be used for implementing the printed transmission line afferent the antenna;
- If a Ground plane is required in line geometry, that plane has to be continuous and sufficiently extended, so the geometry can be as similar as possible to the related canonical model;
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as reference Ground plane for the transmission line;
- It is wise to surround (on both sides) the PCB transmission line with Ground, avoid having other signal tracks facing directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other signal tracks on different layers;
- The ground surrounding the antenna line on PCB has to be strictly connected to the main Ground Plane by means of via holes (once per 2mm at least), placed close to the ground edges facing line track;
- Place EM noisy devices as far as possible from UE910 antenna line;
- Keep the antenna line far away from the UE910 power supply lines;
- If EM noisy devices are present on the PCB hosting the UE910, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If EM noisy devices are not present around the line, the use of geometries like Microstrip or Grounded Coplanar Waveguide has to be preferred, since they typically ensure less attenuation if compared to a Stripline having same length;

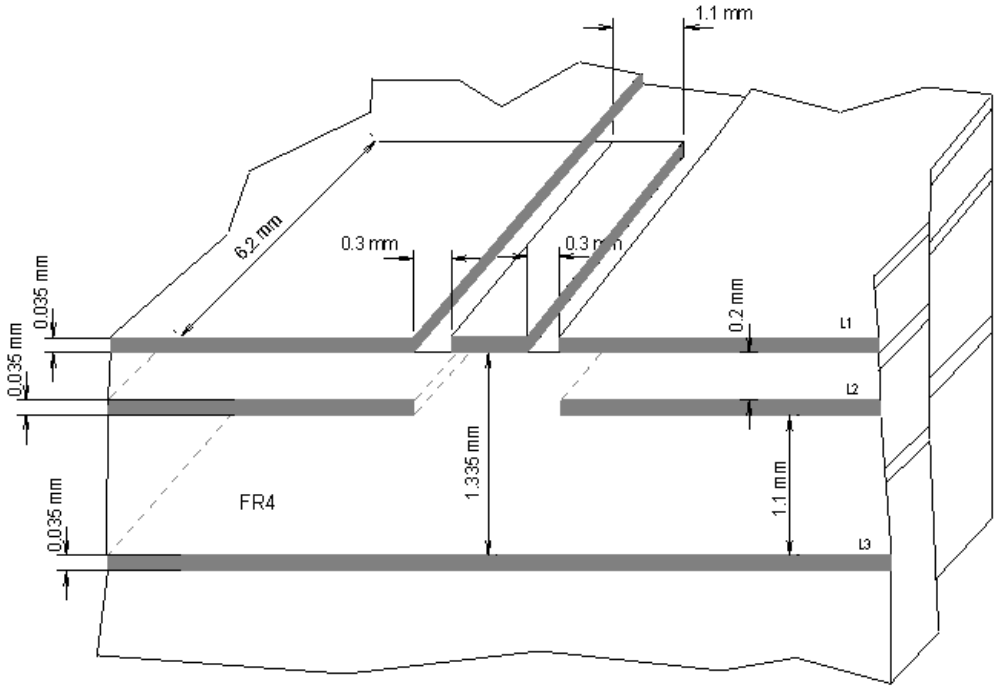
 

# 6.5 PCB Guidelines in case of FCC certification

In the case FCC certification is required for an application using UE910-NAx, according to FCC KDB 996369 for modular approval requirements, the transmission line has to be similar to that implemented on UE910 interface board and described in the following chapter.

## 6.5.1 Transmission line design

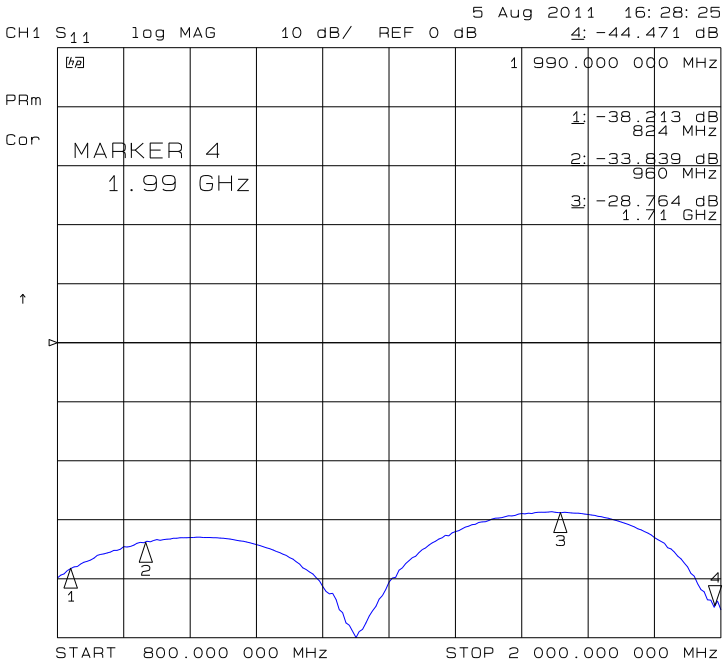
During the design of the UE910 interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.
The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity $\varepsilon_r$ = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.
A characteristic impedance of nearly 50 Ω is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:



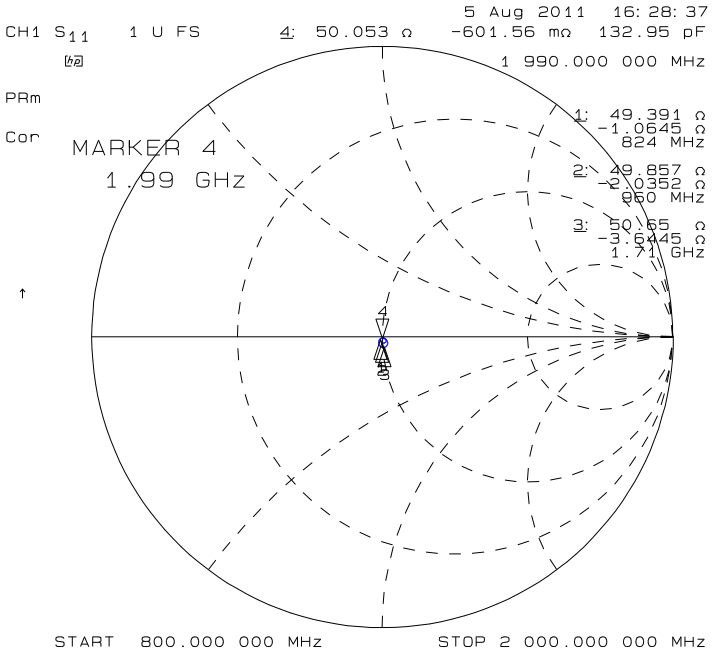
### 6.5.2 Transmission line measurements

HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.

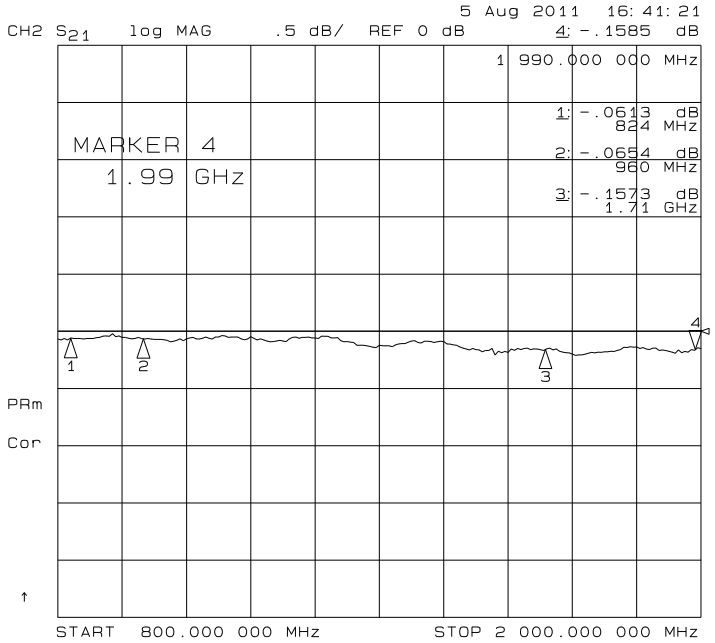
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:




Insertion Loss of G-CPW line plus SMA connector is shown below:



# 6.6 Antenna - Installation Guidelines

Install the antenna in a place covered by the GSM / WCDMA signal.
If the device antenna is located farther than 20cm from the human body and there are no co-located transmitter then the Telit FCC/IC approvals can be re-used by the end product.
If the device antenna is located closer than 20cm from the human body or there are co-located transmitter then the additional FCC/IC testing may be required for the end product (Telit FCC/IC approvals cannot be reused).
Antenna shall not be installed inside metal cases.
Antenna shall be installed also according to antenna manufacturer instructions.

# 7 Logic level specifications

The following table shows the logic level specifications used in the UE910 interface circuits:

**Absolute Maximum Ratings -Not Functional**

| Parameter | Min | Max |
|---|---|---|
| Input level on any digital pin (CMOS 1.8) with respect to ground | -0.3V | 2.1V |
| Input level on any digital pin (CMOS 1.2) with respect to ground | -0.3V | 1.4V |

**Operating Range - Interface levels (1.8V CMOS)**

| Level | Min | Max |
|---|---|---|
| Input high level | 1.5V | 1.9V |
| Input low level | 0V | 0.35V |
| Output high level | 1.6V | 1.9V |
| Output low level | 0V | 0.2V |

**Operating Range - Interface levels (1.2V CMOS)**

| Level | Min | Max |
|---|---|---|
| Input high level | 0.9V | 1.3V |
| Input low level | 0V | 0.3V |
| Output high level | 1V | 1.3V |
| Output low level | 0V | 0.1V |

**Current characteristics**

| Level | Typical |
|---|---|
| Output Current | 1mA |
| Input Current | 1uA |

# 7.1 Unconditional Shutdown

| Signal | Function | I/O | PAD |
|---|---|---|---|
| HW_SHUTDOWN* | Unconditional Shutdown of the Module | I | R13 |

HW_SHUTDOWN* is used to unconditionally shutdown the UE910. Whenever this signal is pulled low, the UE910 is reset. When the device is reset it stops any operation. After the release of the line, the UE910 is unconditionally shut down, without doing any detach operation from the network where it is registered. This behaviour is not a proper shut down because any GSM device is requested to issue a detach request on turn off. For this reason the HW_SHUTDOWN* signal must not be used to normally shutting down the device, but only as an emergency exit in the rare case the device remains stuck waiting for some network response.
The HW_SHUTDOWN* is internally controlled on start-up to achieve always a proper power-on reset sequence, so there's no need to control this pin on start-up.
It may only be used to reset a device already on that is not responding to any command.

**NOTE:**

Do not use this signal to power off the UE910. Use the ON/OFF signal to perform this function or the AT#SHDN command.

**Unconditional Shutdown Signal Operating levels**:

| Signal | Min | Max |
|---|---|---|
| HW_SHUTDOWN* Input high | 1.5V | 1.9V |
| HW_SHUTDOWN* Input low | 0V | 0.35V |

* this signal is internally pulled up so the pin can be left floating if not used.

If unused, this signal may be left unconnected. If used, then it **must always be connected with an open collector transistor**, to permit to the internal circuitry the power on reset and under voltage lockout functions.

# 8 USB Port

The UE910 includes one integrated universal serial bus (USB 2.0 HS) transceiver.

## 8.1 USB 2.0 HS

This port is compliant with the USB 2.0 HS only.
The USB FS is supported for AT interface and data communication.

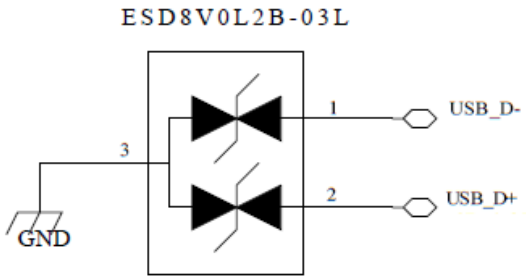
The following table is listing the available signals:

| PAD | Signal | I/O | Function | Type | NOTE |
|---|---|---|---|---|---|
| **B15** | USB_D+ | I/O | USB differential Data (+) | 3.3V | |
| **C15** | USB_D- | I/O | USB differential Data (-) | 3.3V | |
| **A13** | VUSB | AI | Power sense for the internal USB transceiver. | 5V | Accepted range: 4.4V to 5.25V |

The USB_DPLUS and USB_DMINUS signals have a clock rate of 480 MHz.

The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The characteristic impedance value should be as close as possible to 90 Ohms differential.

In case there is a need to add an ESD protection the suggested connection is the following:




**NOTE:**

VUSB pin should be disconnected before activating the Power Saving Mode.

In case of a Firmware upgrade using the USB port, it could be done only using an USB 2.0 HS device.

# 9 SPI port

The UE910 Module is provided by one SPI interface.

The SPI interface defines two handshake lines for flow control and mutual wake-up of the modem and the Application Processor: SRDY (slave ready) and MRDY (master ready).

The AP has the master role, that is, it supplies the clock.

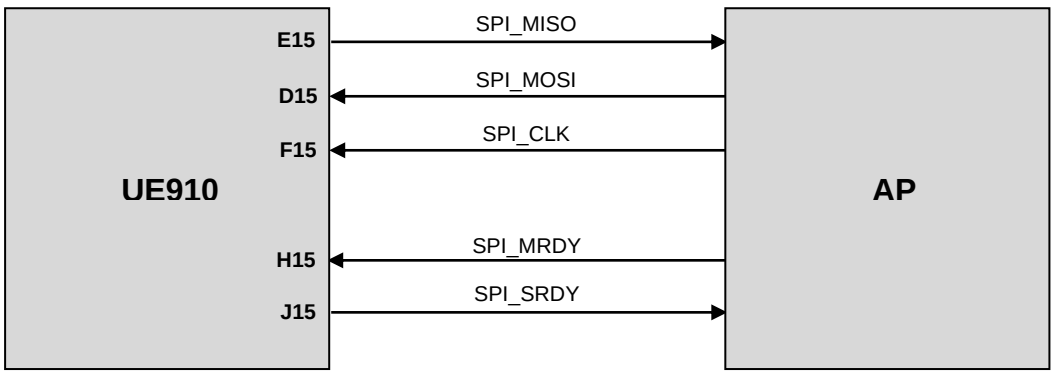
The following table is listing the available signals:

| PAD | Signal | I/O | Function | Type | COMMENT |
|---|---|---|---|---|---|
| D15 | SPI_MOSI | I | SPI MOSI | CMOS 1.8V | Shared with TX_AUX |
| E15 | SPI_MISO | O | SPI MISO | CMOS 1.8V | Shared with RX_AUX |
| F15 | SPI_CLK | I | SPI Clock | CMOS 1.8V | |
| H15 | SPI_MRDY | I | SPI_MRDY | CMOS 1.8V | |
| J15 | SPI_SRDY | O | SPI_SRDY | CMOS 1.8V | |

**NOTE:**

Due to the shared functions, when the SPI port is used, it is not possible to use the AUX_UART port.

## 9.1 SPI Connections



# 10 USB HSIC

The UE910 Module is provided by one USB HSIC interface.
The USB HSIC (High Speed Inter Processor) Interface allows supporting the inter-processor communication between an application processor (AP) – the host, and the modem processor (CP) – the UE910.

The following table is listing the available signals:

| Pad | Signal | Direction | Function | Type | COMMENT |
|---|---|---|---|---|---|
| **A12** | HSIC_USB_DATA | I/O | USB HSIC data signal | CMOS 1.2V | |
| **A11** | HSIC_USB_STRB | I/O | USB HSIC strobe signal | CMOS 1.2V | |
| **H15** | HSIC_SLAVE_WAKEUP | I | Slave Wake Up | CMOS 1.8V | Shared with SPI_MRDY |
| **F15** | HSIC_HOST_WAKEUP | O | Host Wake Up | CMOS 1.8V | Shared with SPI CLK |
| **K15** | HSIC_SUSPEND_REQUEST | O | Slave Suspend Request | CMOS 1.8V | Shared with GPIO08 |
| **J15** | HSIC_HOST_ACTIVE | I | Active Host Indication | CMOS 1.8V | Shared with SPI_SRDY |

For the detailed use of USB HSIC port please refer to the related Application Note.

**NOTE:**

Due to the shared functions, when the USB_HSIC port is used, it is not possible to use the SPI and GPIO_08.

The USB_HSIC is not active by default but it has to be enabled using the AT#PORTCFG command (refer to the AT user guide for the detailed syntax description).

# 11 Serial Ports

The UE910 module is provided with by 2 Asynchronous serial ports:

- MODEM SERIAL PORT 1 (Main)
- MODEM SERIAL PORT 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work.
On the UE910 the ports are CMOS 1.8.

The electrical characteristics of the Serial ports are explained in the following tables:

**Absolute Maximum Ratings -Not Functional**

| Parameter | Min | Max |
|---|---|---|
| Input level on any digital pin (CMOS 1.8) with respect to ground | -0.3V | 2.1V |

**Operating Range - Interface levels (1.8V CMOS)**

| Level | Min | Max |
|---|---|---|
| Input high level | 1.5V | 1.9V |
| Input low level | 0V | 0.35V |
| Output high level | 1.6V | 1.9 |
| Output low level | 0V | 0.2V |

# 11.1 MODEM SERIAL PORT 1 (USIF0)

The serial port 1 on the UE910 is a +1.8V UART with all the 7 RS232 signals.
It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

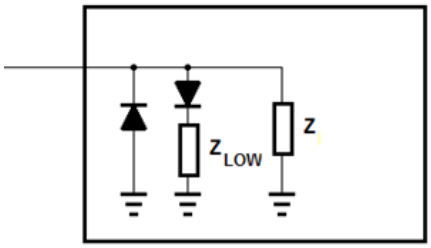
| RS232 Pin # | Signal | UE910 Pad Number | Name | Usage |
|---|---|---|---|---|
| 1 | C109/DCD | **N14** | Data Carrier Detect | Output from the UE910 that indicates the carrier presence |
| 2 | C104/RXD | **M15** | Transmit line *see Note | Output transmit line of UE910 UART |
| 3 | C103/TXD | **N15** | Receive line *see Note | Input receive of the UE910 UART |
| 4 | C108/DTR | **M14** | Data Terminal Ready | Input to the UE910 that controls the DTE READY condition |
| 5 | GND | **M12, B13, P13, E14 …** | Ground | Ground |
| 6 | C107/DSR | **P14** | Data Set Ready | Output from the UE910 that indicates the module is ready |
| 7 | C106/CTS | **P15** | Clear to Send | Output from the UE910 that controls the Hardware flow control |
| 8 | C105/RTS | **L14** | Request to Send | Input to the UE910 that controls the Hardware flow control |
| 9 | C125/RING | **R14** | Ring Indicator | Output from the UE910 that indicates the incoming call condition |

The following table shows the typical input value of internal pull-up resistors for RTS DTR and TXD input lines and in all module states:

| STATE | RTS DTR TXD | |
|---|---|---|
| | | Pull up tied to |
| **ON** | 5K to 12K | 1V8 |
| **OFF** | Schottky diode | |
| **RESET** | Schottky diode | |
| **POWER SAVING** | 5K to 12K | 1V8 |

The input line ON_OFF and RESET state can be treated as in picture below




**NOTE:**

According to V.24, some signal names are referred to the application side, therefore on the UE910 side these signal are on the opposite direction:
TXD on the application side will be connected to the receive line (here named C103/TXD)
RXD on the application side will be connected to the transmit line (here named C104/RXD)

**NOTE:**

For a minimum implementation, only the TXD, RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

# 11.2 MODEM SERIAL PORT 2 (USIF1)

The secondary serial port on the UE910 is a CMOS1.8V with only the RX and TX signals.
The signals of the UE910 serial port are:

| PAD | Signal | I/O | Function | Type | COMMENT |
|---|---|---|---|---|---|
| **D15** | TX_AUX | O | Auxiliary UART (TX Data to DTE) | CMOS 1.8V | SHARED WITH SPI_MTSR |
| **E15** | RX_AUX | I | Auxiliary UART (RX Data from DTE) | CMOS 1.8V | SHARED WITH SPI_MRST |

**NOTE:**

Due to the shared pins, when the Modem Serial port is used, it is not possible to use the SPI functions.

**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

# 11.3 RS232 level translation

In order to interface the UE910 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

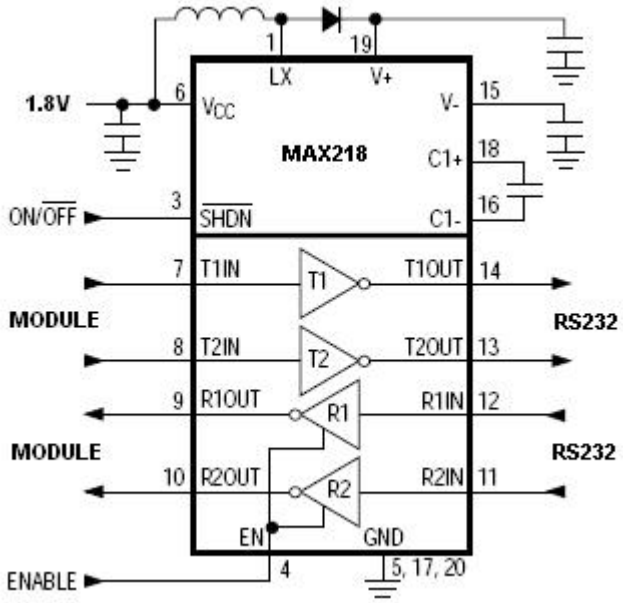
- invert the electrical signal in both directions;
- Change the level from 0/1.8V to +15/-15V.

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).
By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.
In order to translate the whole set of control lines of the UART you will need:

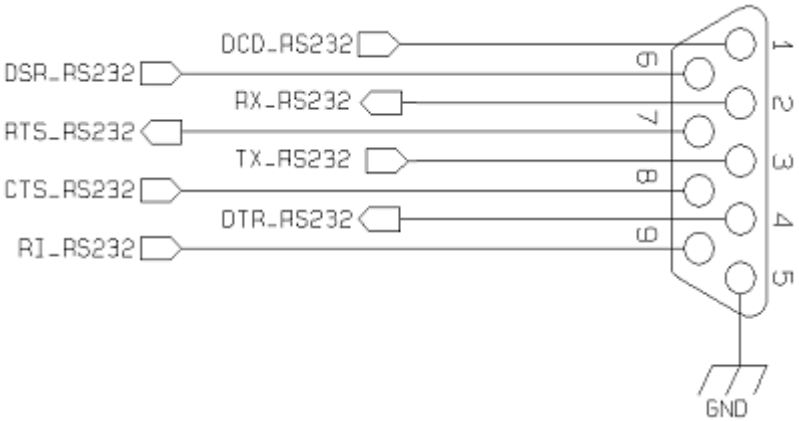
- 5 drivers
- 3 receivers

An example of RS232 level adaptation circuitry could be done using a MAXIM transceiver (MAX218)
In this case the chipset is capable to translate directly from 1.8V to the RS232 levels (Example done on 4 signals only).




The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



# 12 Audio Section Overview

The UE910 is provided by two main interfaces:

- Analog Audio Path
- Digital Audio Path

The UE910 variants supporting the Audio are listed in the following table::

| Product | Audio | Notes |
|---|---|---|
| UE910-EUR | YES | |
| UE910-EUD | NO | Reserved Pads:,B2, B3, B4, B5 |
| UE910-NAR | YES | |
| UE910-NAD | NO | Reserved Pads:,B2, B3, B4, B5 |

**NOTE:**

The two Paths could not be used in parallel; If the Analog Voice lines are selected, the DVI interface is disabled and Vice versa.

## 12.1 Analog Voice Interface

The Base Band Chip of the UE910 provides one differential input for audio to be transmitted (Uplink) and a balanced BTL output for audio to be received (downlink).

The Signals are available on the following Pads:

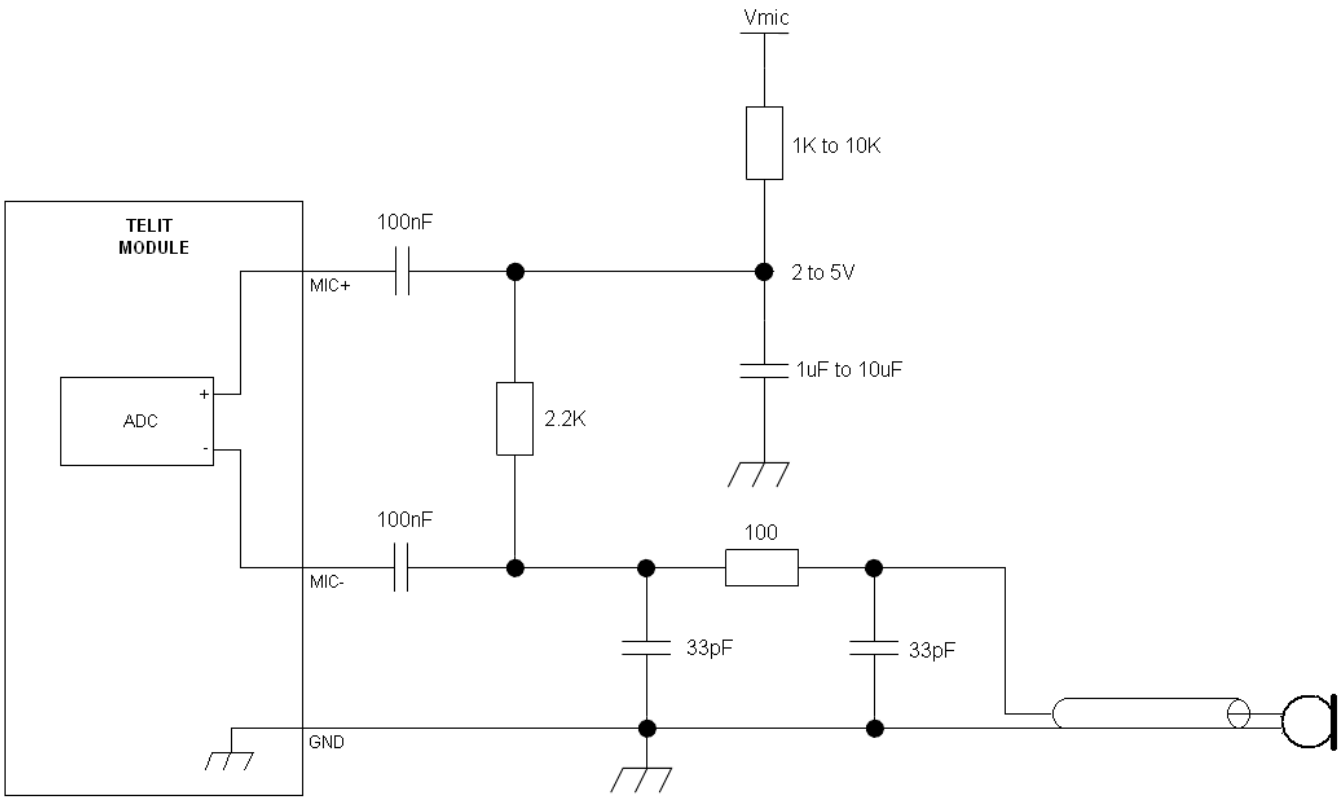
| PAD | Signal | I/O | Function | Note |
|---|---|---|---|---|
| B2 | EAR+ | O | Analog Voice Interface (EAR+) | |
| B3 | EAR- | O | Analog Voice Interface (EAR-) | |
| B4 | MIC+ | I | Analog Voice Interface (MIC+) | |
| B5 | MIC- | I | Analog Voice Interface (MIC-) | |

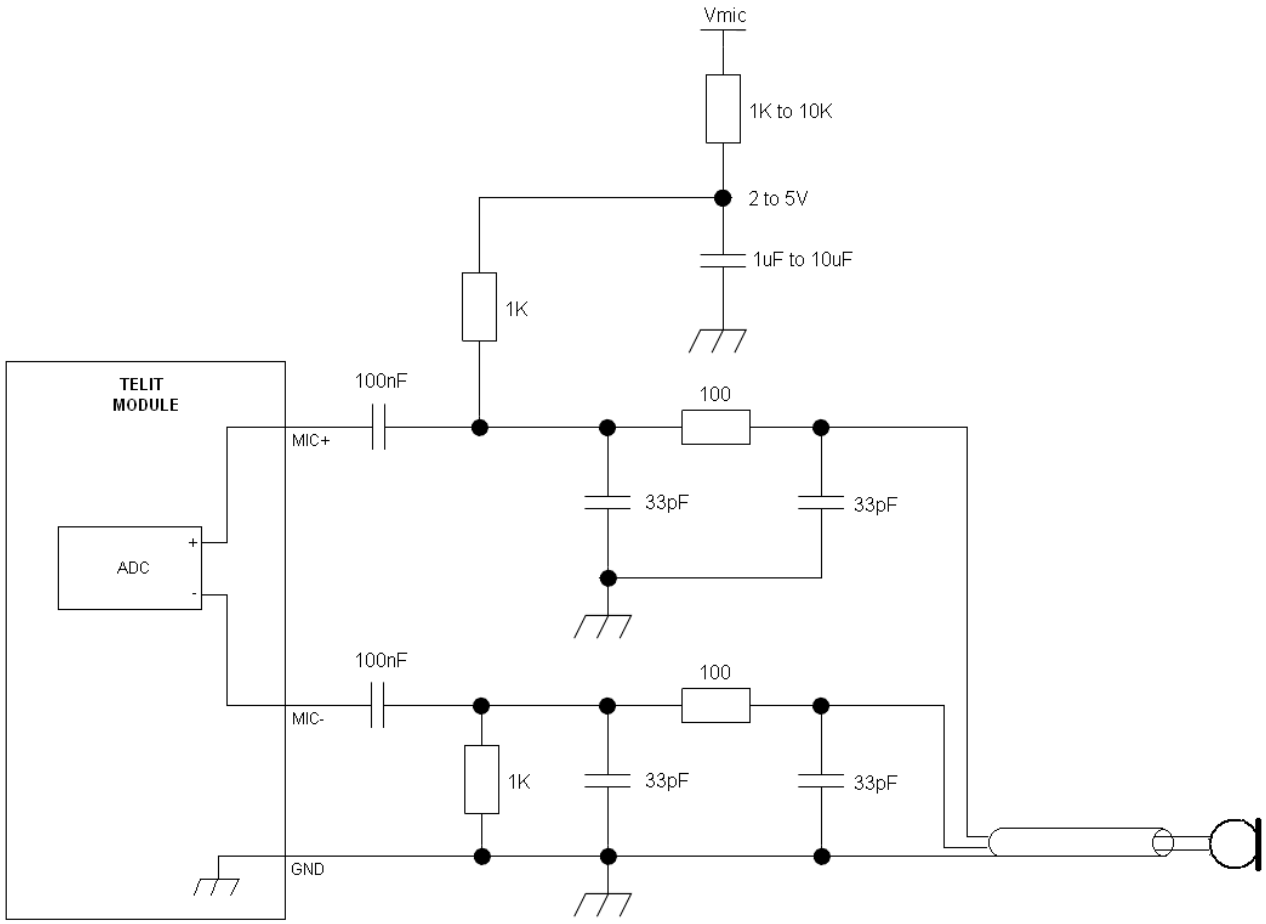
## 12.1.1 MIC connection

The bias for the microphone has to be as clean as possible; the first connection (single ended) is preferable since the Vmic noise and ground noise are fed into the input as common mode and then rejected. This sounds strange; usually the connection to use in order to reject the common mode is the balanced one. In this situation we have to recall that the microphone is a sound to current transducer, so the resistor is the current to tension transducer, so finally the resistor feeds the input in balanced way even if the configuration, from a microphone point of view, seems to be un-balanced.

The following images show some connection examples:

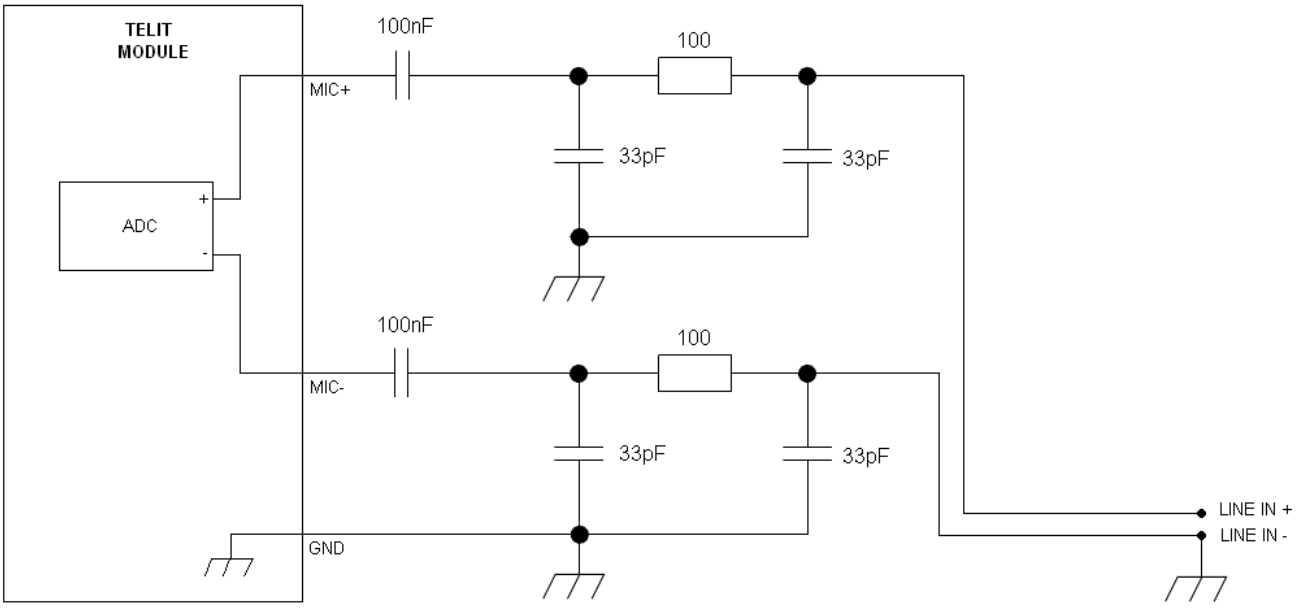


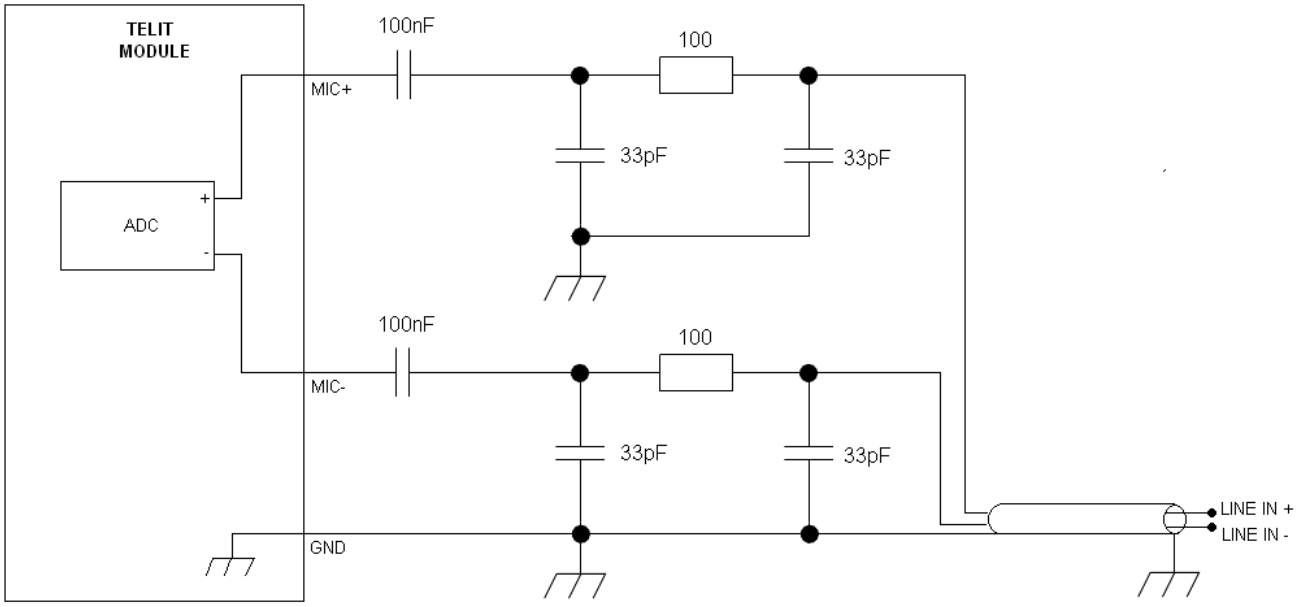
If a "balanced way" is anyway desired, much more care has to be taken to Vmic noise and ground noise; also the 33pF-100Ohm-33pF RF-filter has to be doubled (one each wire).




**TIP:** Since the J-FET transistor inside the microphone acts as RF-detector-amplifier, ask vendor for a microphone with anti-EMI capacitor (usually a 33pF or a 10pF capacitor placed across the output terminals inside the case).

## 12.1.2 LINE IN Connection



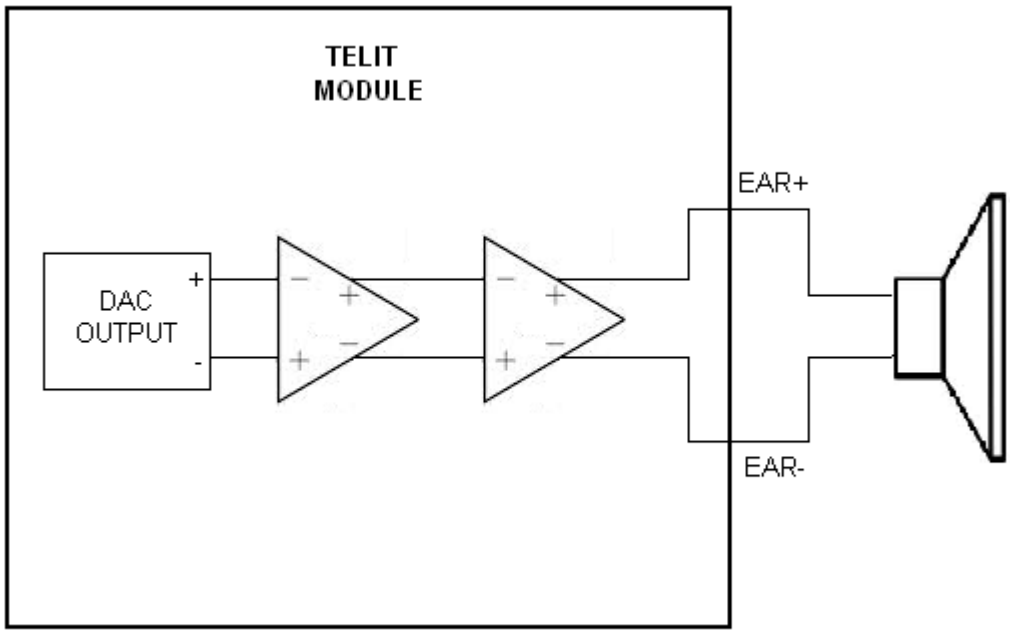




If the audio source is not a mike but a different device, the following connections can be done.
Place 100nF capacitor in series with both inputs, so the DC current is blocked.
Place the 33pF-100Ohm-33pF RF-filter, in order to prevent some EMI field to get into the high impedance high gain MIC inputs.
Since the input is differential, the common mode voltage noise between the two (different) ground is rejected, provided that both MIC+ & MIC- are connected directly onto the source.

## 12.1.3 EAR Connection

The audio output of the UE910 is balanced, this is helpful to double the level and to reject common mode (click and pop are common mode and therefore rejected).
These outputs can drive directly a small loudspeaker with electrical impedance not lower than 16 Ohm.




**TIP:** in order to get the maximum audio level at a given output voltage level (dBspl/Vrms), the following breaking through procedure can be used. Have the loudspeaker as close as you can to the listener (this simplify also the echo cancelling); choose the loudspeaker with the higher sensitivity (dBspl per W); choose loudspeakers with the impedance close to the limit, in order to feed more power inside the transducer (it increases the W/Vrms ratio). If this were not enough, an external amplifier should be used.

## 12.1.4 Electrical Characteristics

### 12.1.4.1 Input Lines

| Microphone/Line-in path | |
|---|---|
| Line Type | Differential |
| Coupling capacitor | ≥ 100nF |
| Differential input resistance | 10kΩ |
| **Levels** | |
| To have 0dBm0 @1KHz *(*)* | Differential input voltage |
| AT#HFMICG=0 | 247mVrms |
| AT#HFMICG=1 (+3dB) | 175mVrms |
| AT#HFMICG=2 (+6dB) | 124mVrms |
| AT#HFMICG=3 (+9dB) | 88mVrms |
| AT#HFMICG=4 (+12dB) | 62mVrms |
| AT#HFMICG=5 (+15dB) | 44mVrms |
| AT#HFMICG=6 (+18dB) | 31mVrms |
| AT#HFMICG=7 (+21dB) | 22mVrms |
| AT#HFMICG=8 (+24dB) | 16mVrms |
| AT#HFMICG=9 (+27dB) | 11mVrms |
| AT#HFMICG=10 (+30dB) | 8mVrms |
| AT#HFMICG=11 (+33dB) | 6mVrms |
| AT#HFMICG=12 (+36dB) | 4mVrms |
| AT#HFMICG=13 (+39dB) | 3mVrms |
| AT#HFMICG=14 (+42dB) | 2mVrms |

*(*)* 0 dBm0 in the network are -3.14 dBfs

**TIP:** The Electret microphone is internally amplified by a J-FET transistor, thus the sound is carried out as saturation drain current; this means that the Norton equivalence has to be considered. The signal is converted to voltage on the 2.2KOhm resistance, from there on circuitry has to be routed in order to not pick up common mode noise; beware of the return path (ground).

### 12.1.4.2 Output Lines

| EAR/Line-out Output | |
|---|---|
| output load resistance | ≥ 8 Ω |
| signal bandwidth | 250÷3400Hz<br>*(@ -3dB with default filter)* |
| differential output voltage | $1V_{rms}$ *@ 0dBfs (*)* |
| volume | -20÷0 dB step ~ 2dB |

*(*)* in default condition: AT+CLVL=10,

**TIP:**

We suggest driving the load differentially; this kills all the common mode noises (click and pop, for example), the output swing will double (+6dB) and the big output coupling capacitor will be avoided.

However if particular OEM application needs, also a Single Ended *(S.E)* circuitry can be implemented. The OEM circuitry shall be designed to reduce the common mode noise typically generated by the return path of the big currents.

In order to get the maximum power output from the device, the resistance of the tracks has to be negligible in comparison to the load.

**NOTES:**

For more information refer to Telit document: "80000NT10007a Audio Settings Application Note".

# 12.2 Digital Voice Interface

The UE910 Module is provided by one DVI digital audio interface.

## 12.2.1 Electrical Characteristics

The product is providing the Digital Voice Interface (DVI) on the following Pins:

| Digital Voice Interface (DVI) | | | | | |
|---|---|---|---|---|---|
| **PAD** | **Signal** | **I/O** | **Function** | **Note** | **Type** |
| **B9** | DVI_WA0 | I/O | Digital Voice Interface (Word Alignment / LRCLK) | | CMOS 1.8V |
| **B6** | DVI_RX | I | Digital Voice Interface (RX) | | CMOS 1.8V |
| **B7** | DVI_TX | O | Digital Voice Interface (TX) | | CMOS 1.8V |
| **B8** | DVI_CLK | I/O | Digital Voice Interface (BCLK) | | CMOS 1.8V |

## 12.2.2 CODEC Examples

Please refer to the Digital Audio Application note.

# 13 General Purpose I/O

The UE910 module is provided by a set of Digital Input / Output pins

Input pads can only be read; they report the digital value (high or low) present on the pad at the read time.
Output pads can only be written or queried and set the value of the pad output.
An alternate function pad is internally controlled by the UE910 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the UE910:

| PAD | Signal | I/O | Function | Type | Drive strength | Default State | Note |
|---|---|---|---|---|---|---|---|
| **C8** | GPIO_01 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | Alternate function STAT LED |
| **C9** | GPIO_02 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |
| **C10** | GPIO_03 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |
| **C11** | GPIO_04 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |
| **B14** | GPIO_05 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |
| **C12** | GPIO_06 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |
| **C13** | GPIO_07 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |
| **K15** | GPIO_08 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |
| **L15** | GPIO_09 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |
| **G15** | GPIO_10 | I/O | Configurable GPIO | CMOS 1.8V | **1** mA | INPUT | |

# 13.1 GPIO Logic levels

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels.
The following table shows the logic level specifications used in the UE910 interface circuits:

**Absolute Maximum Ratings -Not Functional**

| Parameter | Min | Max |
|---|---|---|
| Input level on any digital pin (CMOS 1.8) with respect to ground | -0.3V | 2.1V |

**Operating Range - Interface levels (1.8V CMOS)**

| Level | Min | Max |
|---|---|---|
| Input high level | 1.5V | 1.9V |
| Input low level | 0V | 0.35V |
| Output high level | 1.6V | 1.9 |
| Output low level | 0V | 0.2V |

## 13.2 Using a GPIO Pad as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.
If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 1.8V.

**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE910 when the module is powered off or during an ON/OFF transition.

## 13.3 Using a GPIO Pad as OUTPUT

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

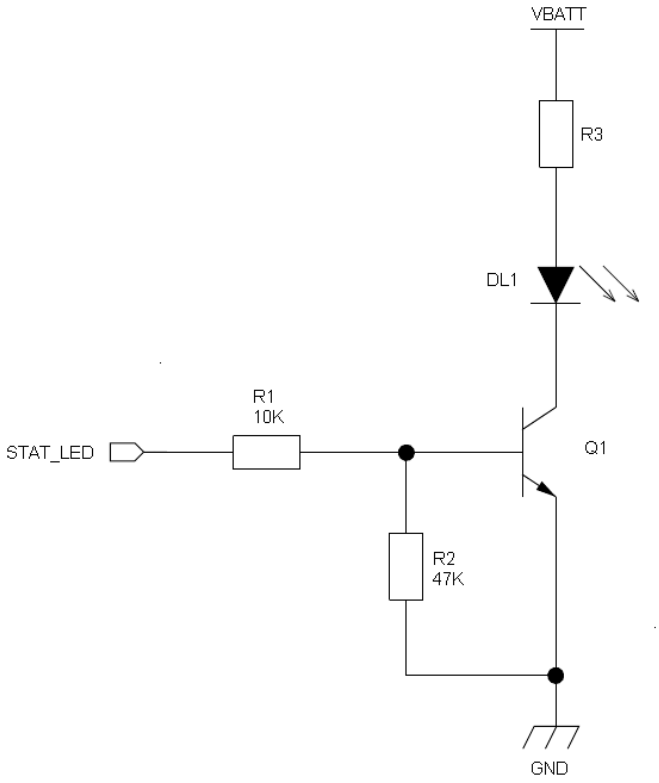
 

# 13.4 Indication of network service availability

The STAT_LED pin status shows information on the network service availability and Call status. The function is available as alternate function of GPIO_01 (to be enabled using the AT#GPIO=1,0,2 command).
In the UE910 modules, the STAT_LED needs an external transistor to drive an external LED. Therefore, the status indicated in the following table is reversed with respect to the pin status.

| Device Status | LED status |
|---|---|
| Device off | Permanently off |
| Not Registered | Permanently on |
| Registered in idle | Blinking 1sec on + 2 sec off |
| Registered in idle + power saving | It depends on the event that triggers the wakeup (In sync with network paging) |
| Voice Call Active | Permanently on |
| Dial-Up | Blinking 1 sec on + 2 sec off |

A schematic example could be:




## 13.5 RTC Bypass out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.
To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. NO Devices must be powered from this pin.

In order to keep the RTC active when VBATT is not supplied it is possible to back up the RTC section connecting a **backup circuit** to the related VRTC signal (pad C14 on module's Pinout).

For additional details on the Backup solutions please refer to the related application note (xE910 RTC Backup Application Note)

## 13.6 External SIM Holder Implementation

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).

## 13.7 VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module.
The signal is present on Pad R11 and it is in common with the PWRMON (module powered ON indication) function.
This output is always active when the module is powered ON.

The operating range characteristics of the supply are:

| Level | Min | Typical | Max |
|---|---|---|---|
| Output voltage | 1.78V | 1.80V | 1.82V |
| Output current | - | - | 60mA |
| Output bypass capacitor (inside the module) | | 1uF | |

# 13.8 ADC Converter

## 13.8.1 Description

The UE910 is provided by one AD converter. It is able to read a voltage level in the range of 0÷1.2 volts applied on the ADC pin input, store and convert it into 10 bit word.
The following table is showing the ADC characteristics:

| | Min | Typical | Max | Units |
|---|---|---|---|---|
| Input Voltage range | 0 | - | 1.2 | Volt |
| AD conversion | - | - | 10 | bits |
| Input Resistance | 1 | - | - | Mohm |
| Input Capacitance | - | 1 | - | pF |

The input line is named as **ADC_IN1** and it is available on Pad **B1**

## 13.8.2 Using ADC Converter

An AT command is available to use the ADC function.

The command is ***AT#ADC=1,2***

The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

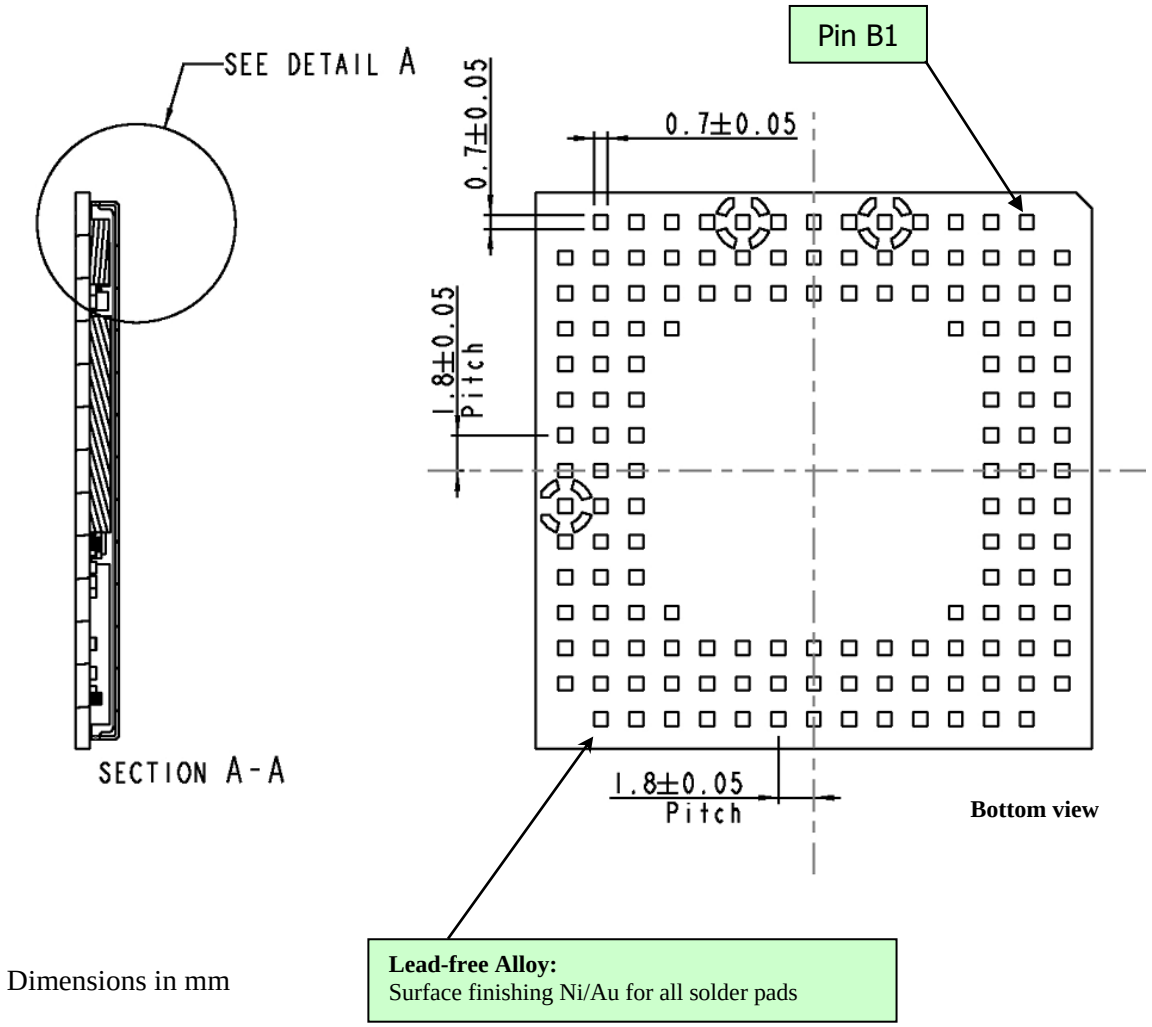
 

# 14 Mounting the UE910 on the application

## 14.1 General

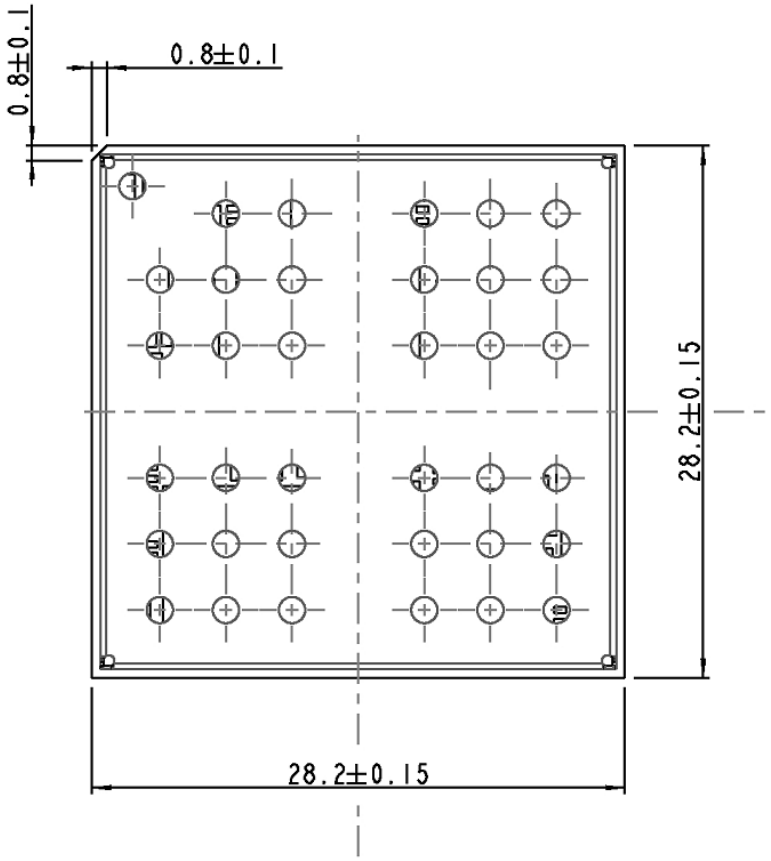
The UE910 modules have been designed in order to be compliant with a standard lead-free SMT process.

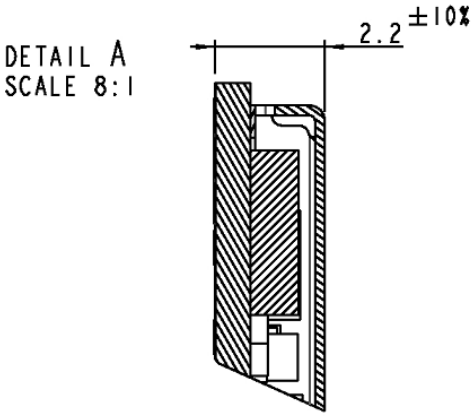
## 14.2 Module finishing & dimensions



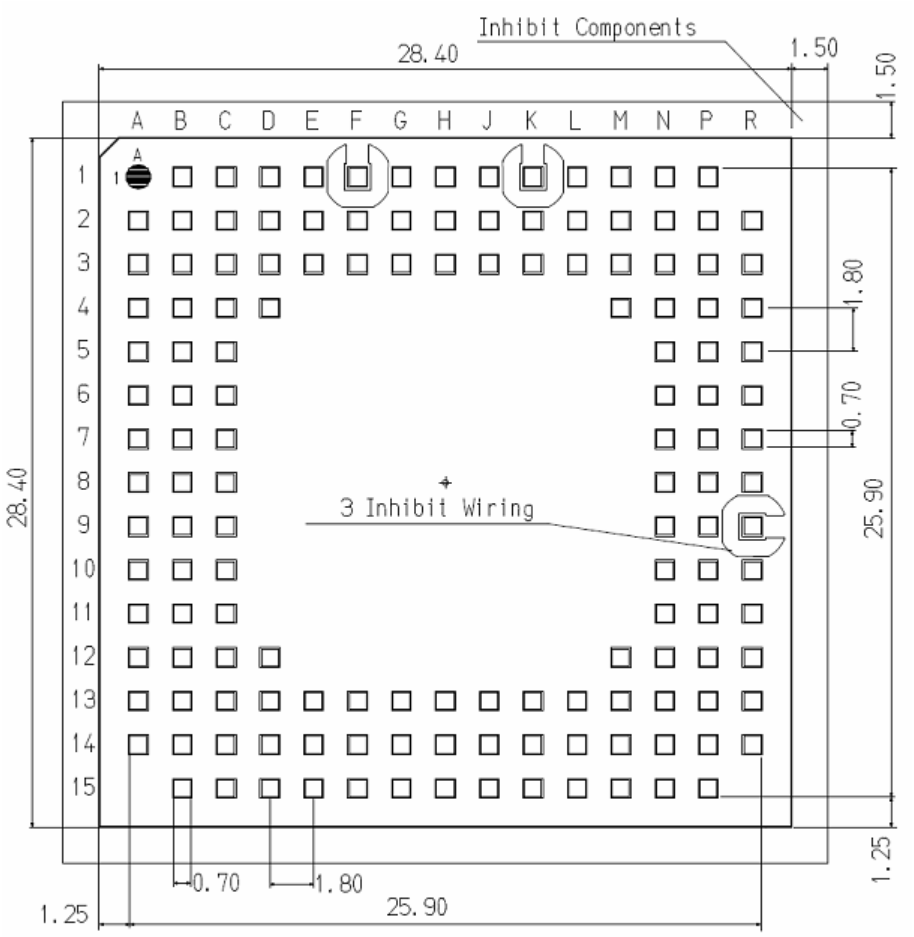

Dimensions in mm


0.8±0.1
0.8±0.1
28.2±0.15
28.2±0.15


DETAIL A
SCALE 8:1
2.2 ±10%

# 14.3 Recommended foot print for the application




**TOP VIEW**

In order to easily rework the UE910 is suggested to consider on the application a 1.5 mm placement inhibit area around the module.
It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

**NOTE:**

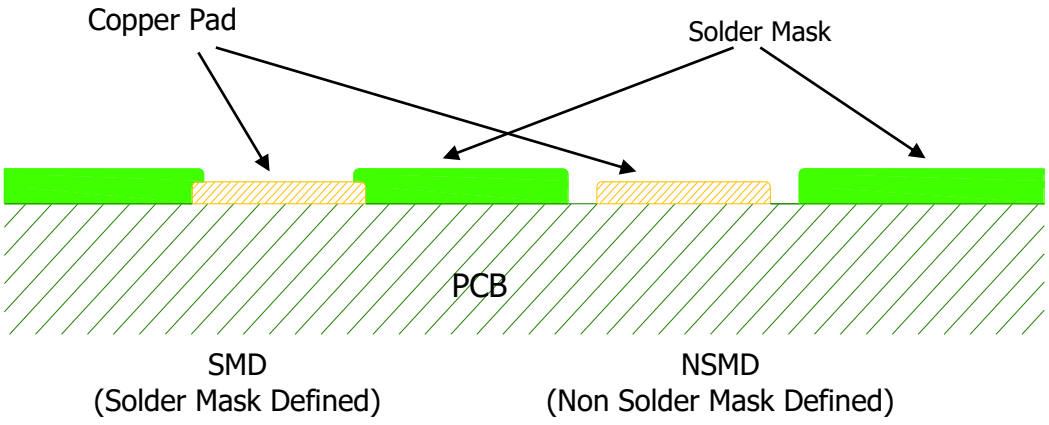
In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

## 14.4 Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

## 14.5 PCB pad design

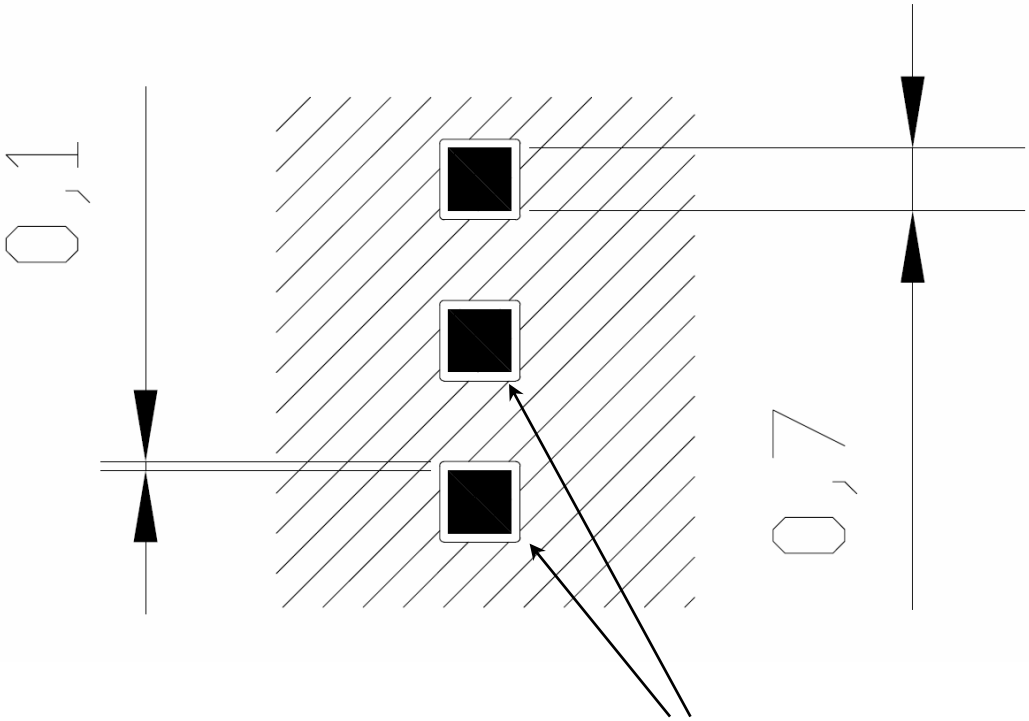
Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



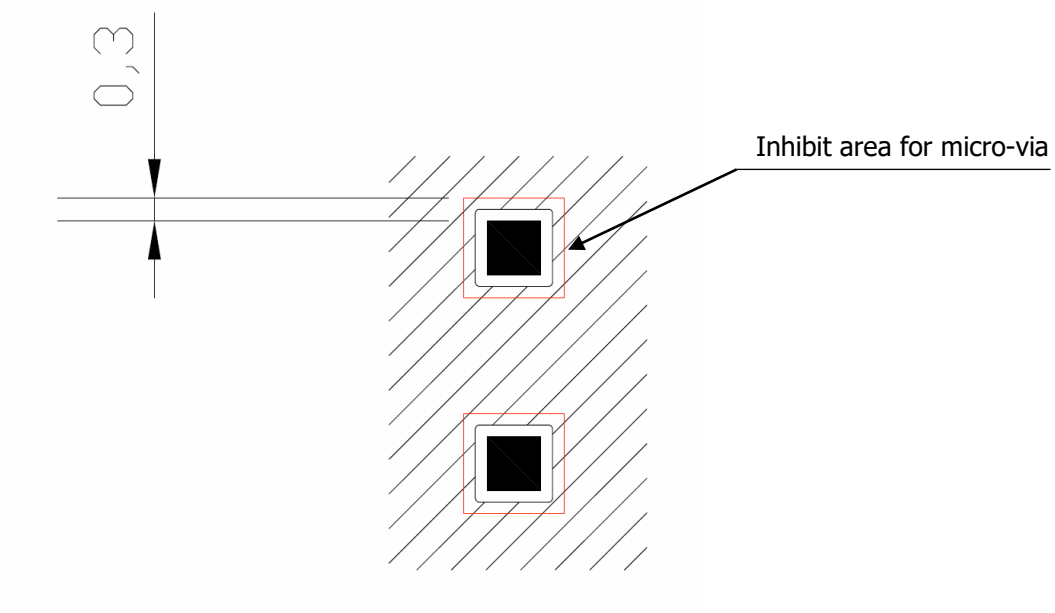

 

## 14.6 PCB pad dimensions

The recommendation for the PCB pads dimensions are described in the following image (dimensions in mm)



It is not recommended to place via or micro-via not covered by solder resist in an area of 0,3 mm around the pads unless it carries the same signal of the pad itself (see following figure).




Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

| Finish | Layer thickness [µm] | Properties |
|---|---|---|
| Electro-less Ni / Immersion Au | 3 –7 / 0.05 – 0.15 | good solder ability protection, high shear force values |

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.
It is not necessary to panel the application's PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

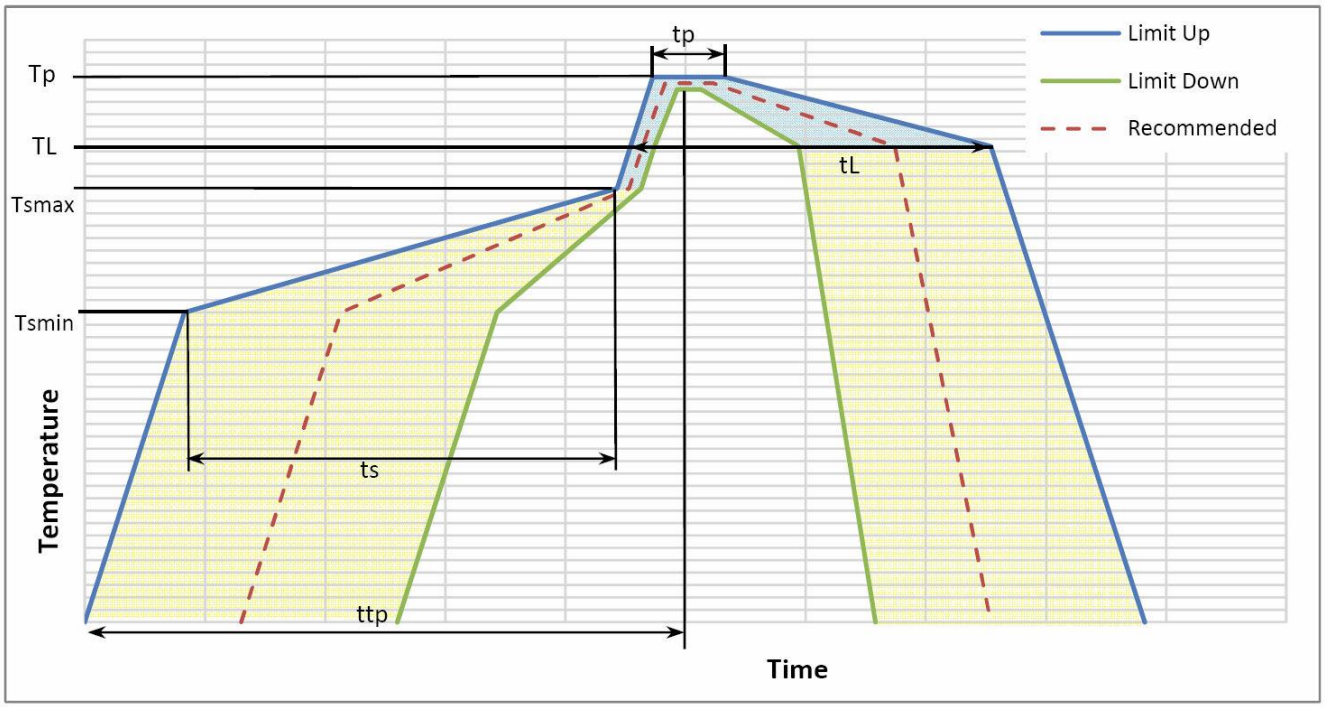
# 14.7 Solder paste

| | Lead free |
|---|---|
| **Solder paste** | Sn/Ag/Cu |
| | |

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

## 14.7.1 UE910 Solder reflow

Recommended solder reflow profile:



| Profile Feature | Pb-Free Assembly |
|---|---|
| Average ramp-up rate ($T_L$ to $T_P$) | 3°C/second max |
| Preheat<br>– Temperature Min (Tsmin)<br>– Temperature Max (Tsmax)<br>– Time (min to max) (ts) | <br>150°C<br>200°C<br>60-180 seconds |
| Tsmax to TL<br>– Ramp-up Rate | <br>3°C/second max |
| Time maintained above:<br>– Temperature (TL)<br>– Time (tL) | <br>217°C<br>60-150 seconds |
| Peak Temperature (Tp) | 245 +0/-5°C |
| Time within 5°C of actual Peak Temperature (tp) | 10-30 seconds |
| Ramp-down Rate | 6°C/second max. |
| Time 25°C to Peak Temperature | 8 minutes max. |

**NOTE:**

All temperatures refer to topside of the package, measured on the package body surface

**WARNING:**

The UE910 module withstands one reflow process only.

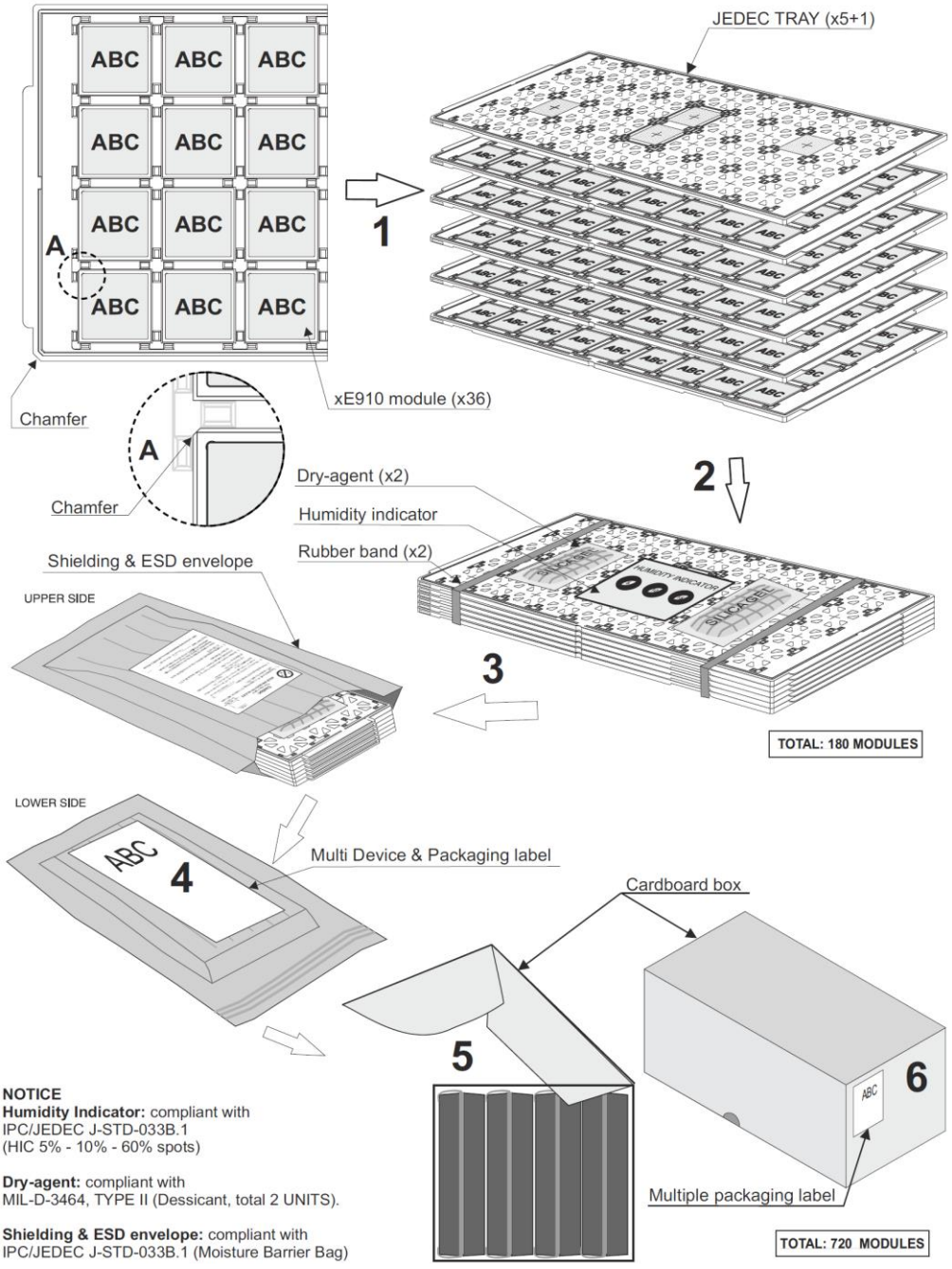
**WARNING:**

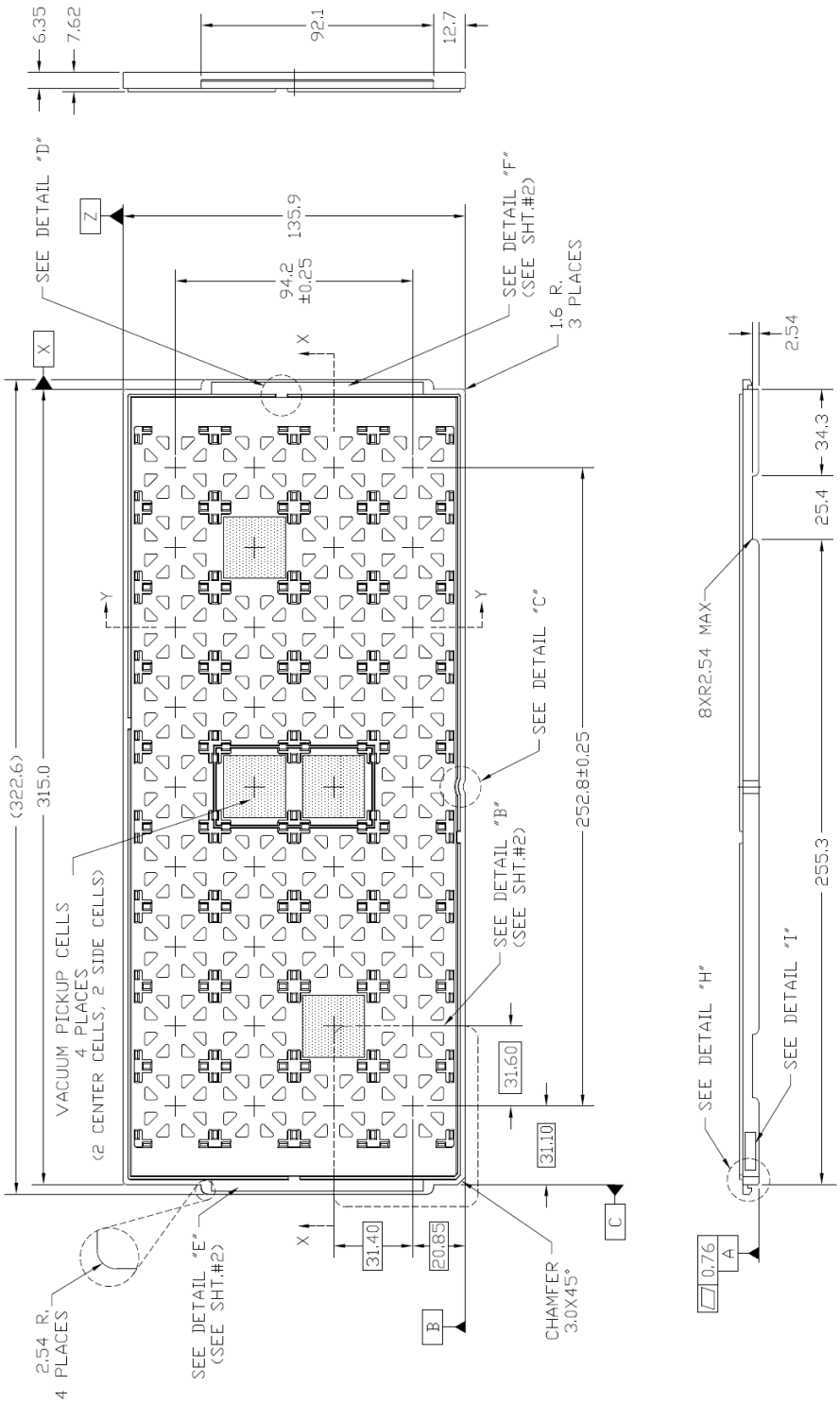
The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage.

# 14.8 Packing system (Tray)

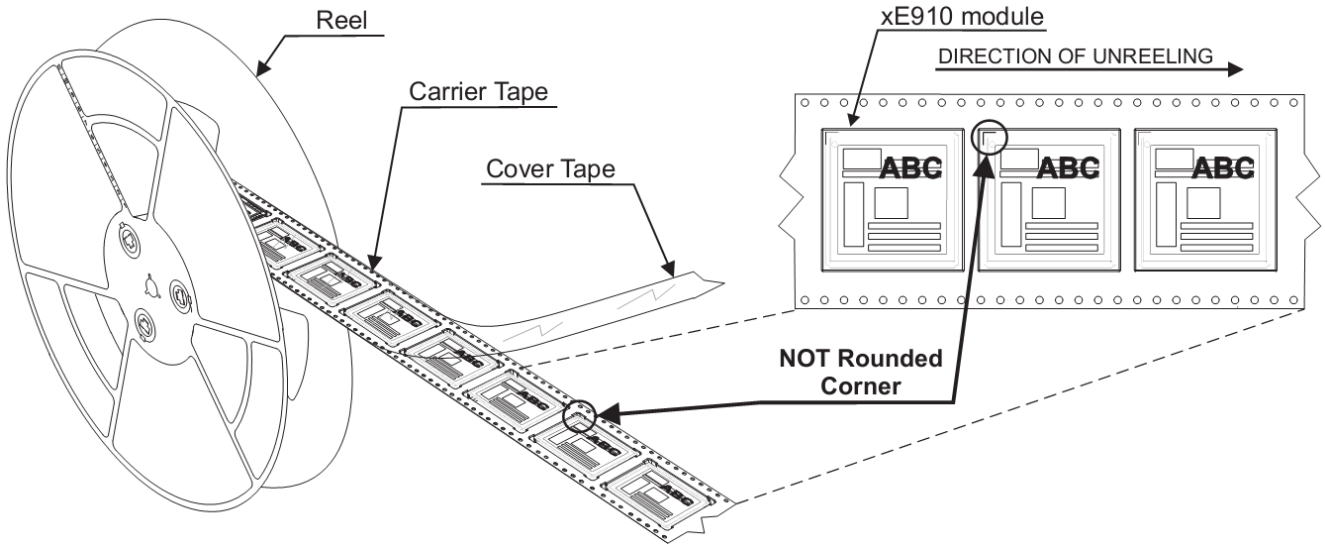
The UE910 modules are packaged on trays of 36 pieces each. These trays can be used in SMT processes for pick & place handling.



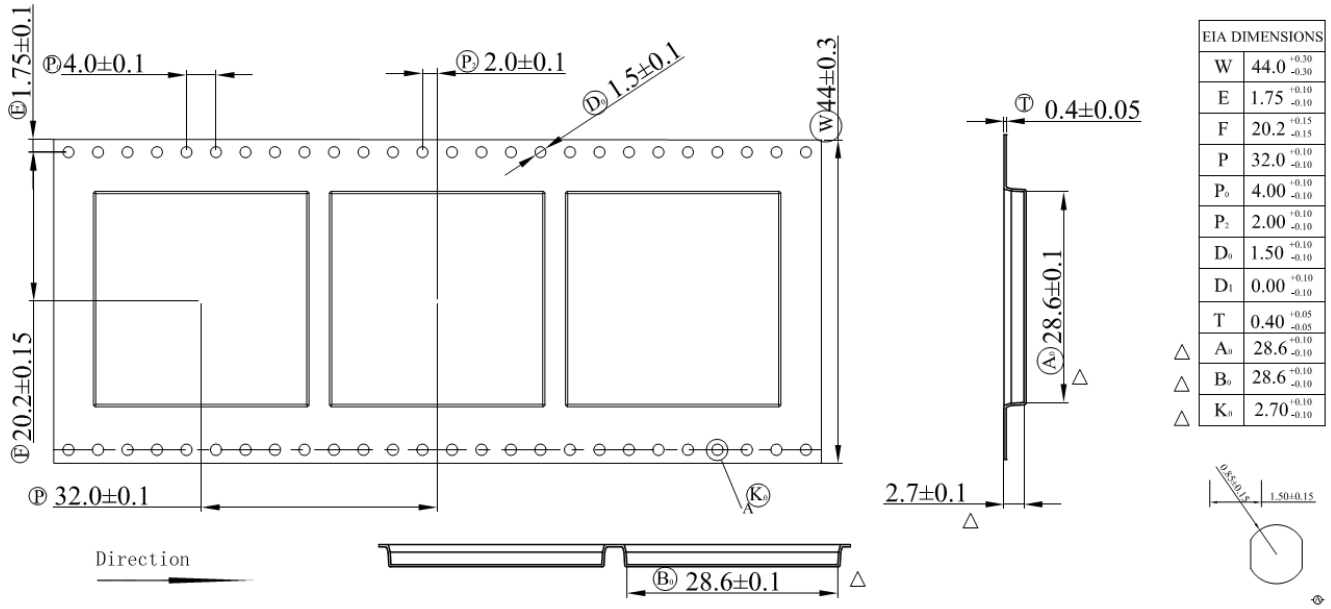


6.35
7.62
92.1
12.7
SEE DETAIL "D"
Z
135.9
94.2 ±0.25
SEE DETAIL "F" (SEE SHT.#2)
1.6 R, 3 PLACES
X
Y
(322.6)
315.0
VACUUM PICKUP CELLS 4 PLACES (2 CENTER CELLS, 2 SIDE CELLS)
SEE DETAIL "C"
252.8±0.25
SEE DETAIL "B" (SEE SHT.#2)
31.60
31.10
C
31.40
20.85
B
CHAMFER 3.0X45°
2.54 R, 4 PLACES
SEE DETAIL "E" (SEE SHT.#2)
2.54
34.3
25.4
8XR2.54 MAX
255.3
SEE DETAIL "H"
SEE DETAIL "I"
0.76
A

# 14.9 Packing System (Reel)

The UE910 can be packaged on reels of 200 pieces each.
See figure for module positioning into the carrier.



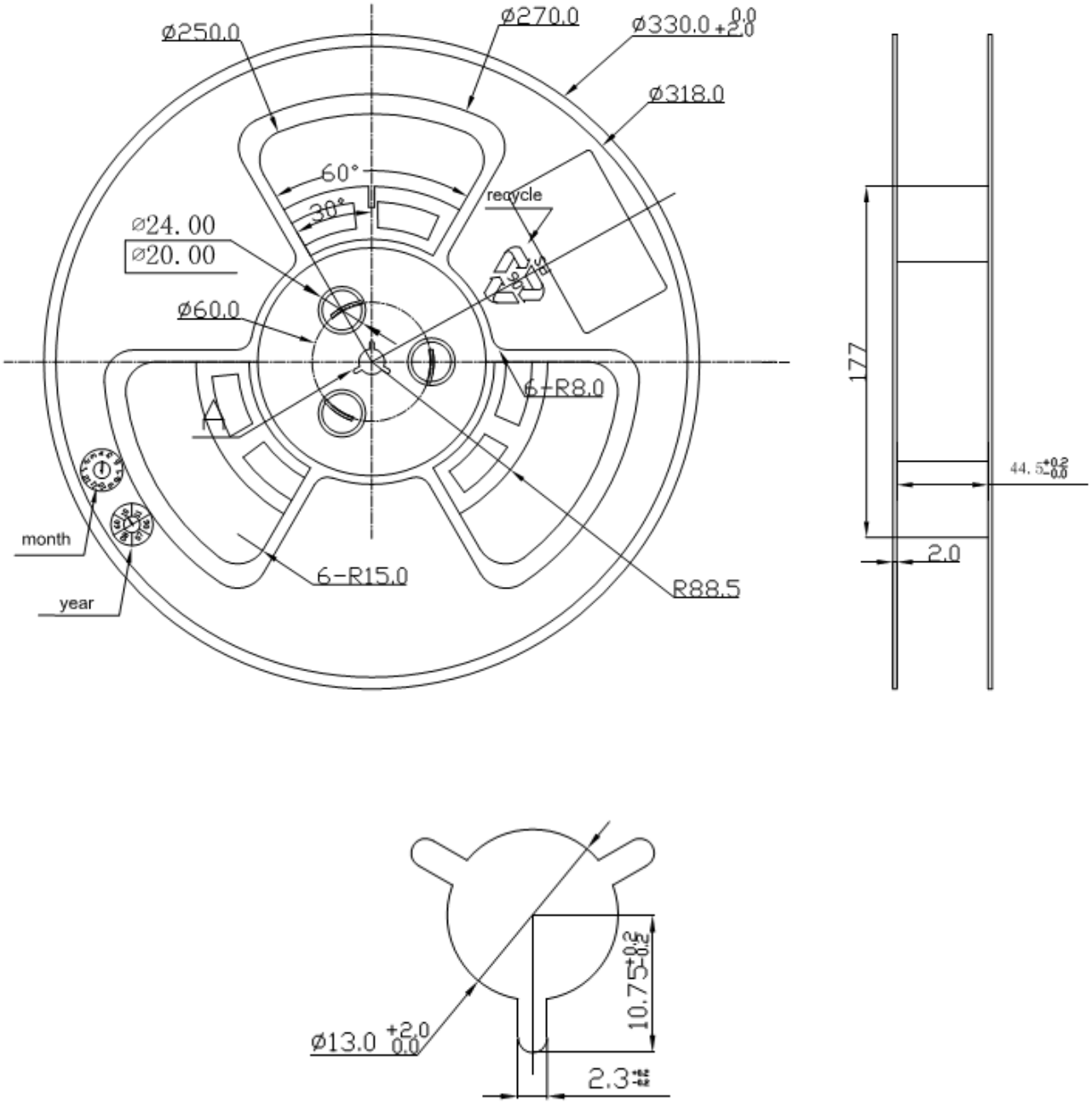

## 14.9.1 Carrier Tape Detail



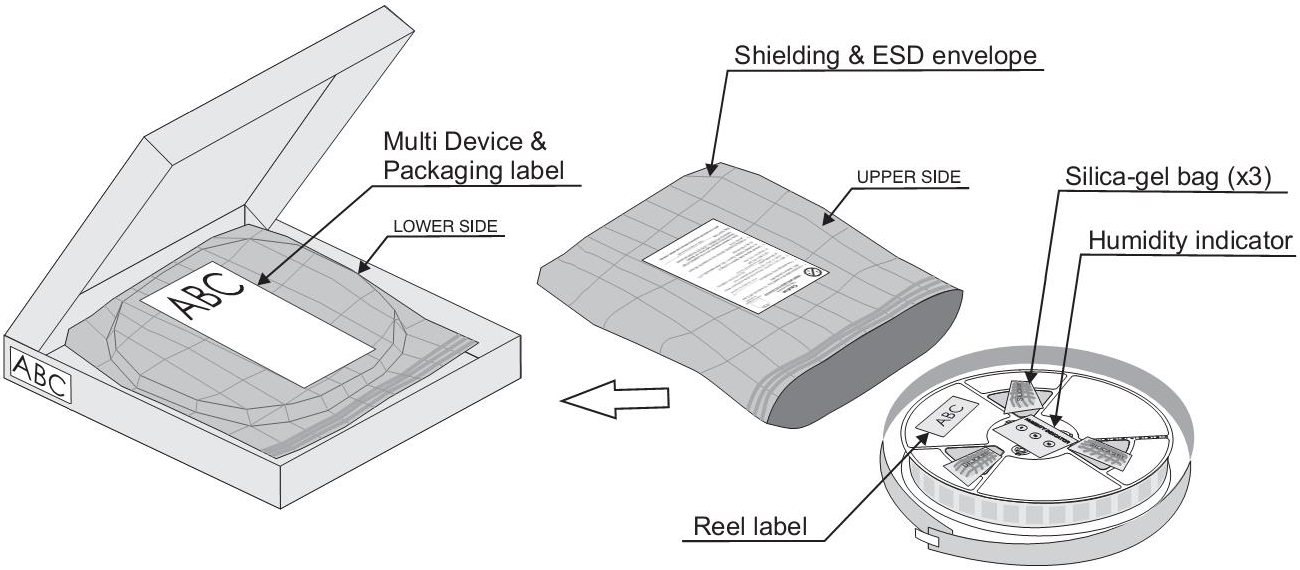

| EIA DIMENSIONS | |
|---|---|
| W | 44.0 +0.30 -0.30 |
| E | 1.75 +0.10 -0.10 |
| F | 20.2 +0.15 -0.15 |
| P | 32.0 +0.10 -0.10 |
| $P_0$ | 4.00 +0.10 -0.10 |
| $P_2$ | 2.00 +0.10 -0.10 |
| $D_0$ | 1.50 +0.10 -0.10 |
| $D_1$ | 0.00 +0.10 -0.10 |
| T | 0.40 +0.05 -0.05 |
| $A_0$ | 28.6 +0.10 -0.10 |
| $B_0$ | 28.6 +0.10 -0.10 |
| $K_0$ | 2.70 +0.10 -0.10 |

## 14.9.2 Reel Detail



### 14.9.3 Packaging Detail




## 14.10 Moisture sensitivity

The UE910 is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:
a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).
b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

# 15 SAFETY RECOMMANDATIONS

**READ CAREFULLY**

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc
- Where there is risk of explosion such as gasoline stations, oil refineries, etc

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the radio equipment introduced on the market.

All the relevant information's are available on the European Community website:

https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/rtte_en

The text of the Directive 2014/53/EU regarding radio equipment is available at:

http://eur-lex.europa.eu/legal-content/EN/TXT/?qid=1429097565265&uri=CELEX:32014L0053

# 16 Conformity assessment issues

## 16.1 FCC/IC Regulatory notices

**Modification statement**

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

*Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.*

**Interference statement**

This device complies with Part 15 of the FCC Rules and Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

*Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.*

**Wireless notice**

This equipment complies with FCC and IC radiation exposure limits set forth for an uncontrolled environment. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body. Antenna gain must be below:

| Frequency band | UE910-NAR, UE910-NAD |
|---|---|
| GSM 850/FDD V | *10.00 dBi* |
| PCS 1900/FDD II | *9.31 dBi* |

| Frequency band | UE910-GL |
|---|---|
| GSM 850/FDD V | *4.14 dBi* |
| PCS 1900/FDD II | *3.04 dBi* |

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

*Cet appareil est conforme aux limites d'exposition aux rayonnements de la IC pour un environnement non contrôlé. L'antenne doit être installé de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps. Gain de l'antenne doit être ci-dessous:*

| ***Bande de fréquence*** | ***UE910-NAR, UE910-NAD*** |
|---|---|
| *GSM 850/FDD V* | *10.00 dBi* |
| *PCS 1900/FDD II* | *9.31 dBi* |

| **Frequency band** | **UE910-GL** |
|---|---|
| GSM 850/FDD V | *4.14 dBi* |
| PCS 1900/FDD II | *3.04 dBi* |

*L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.*

**FCC Class B digital device notice**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

**Labelling Requirements for the Host device**

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Contains FCC ID: RI7UE910NA
Contains IC: 5131A-UE910NA

*L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le FCC ID et le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme suit :*

*Contains FCC ID: RI7UE910NA*
*Contient IC: 5131A-UE910NA*

**CAN ICES-3 (B) / NMB-3 (B)**

This Class B digital apparatus complies with Canadian ICES-003.

*Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.*

# 16.2 ANATEL Regulatory notices

**UE910-GL Homologation #: 08832-17-02618**