NL865H2
Hardware Design Guide

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TECHNICAL
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- NL865H2-W1

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1. INTRODUCTION

1.1. Scope

This document introduces the Telit NL865H2 modules and presents possible and recommended hardware solutions for developing a product based on this module. All the features and solutions detailed in this document are applicable to all NL865H2 variants, where NL865H2 refers to the variants listed in the applicability table.

Obviously, this document cannot embrace every hardware solution or every product that can be designed. Where the suggested hardware configurations need not be considered mandatory, the information given should be used as a guide and a starting point for properly developing your product with the Telit module.

1.2. Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using the Telit module.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

- AT Commands User Guide, 1VV0301611
- NL865H2 TLB Documentation, 1VV0301629

2. GENERAL PRODUCT DESCRIPTION

2.1. Overview

The NL865H2 is part of a new generation of modules in Telit's NBIoT module portfolio.

With its compact LGA footprint, it is designed for those m2m applications requiring miniature foot print.

It is a multi band LTE NBIoT communication product based on the market' latest NBIoT core which allows integrators to plan on availability for even the longest lifecycle applications, highly recommended for new designs specified for NBIoT coverage worldwide.

It is highly recommended for new designs requiring NBIoT coverage in a small and robust LGA package, which implies easy integration and low impact on final application size and costs. Ease of production and small foot print makes it the ideal solution for applications in security alarms, automated meter reading, and pos terminals.

The NL865H2 operates with 1.8 V GPIOs, minimizing power consumption and making it even more ideally suited for battery powered and wearable device applications.

2.2. Product Variants and Frequency Bands

Product	2G Band (MHz)	3G Band (MHz)	4G Band (MHz)	Region
NL865H2-W1	-	-	B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B28, B66, B71, B85	Worldwide

Refer to "RF Section" for details information about frequencies and bands.

NOTE:

The module is supporting the Multi-Frequency Band Indicator (MFBI)

2.3. Target market

NL865H2 can be used for telematics applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are required, for example:

- Telematics services
- Road pricing
- Pay-as-you-drive insurance
- Stolen vehicles tracking
- Internet connectivity

2.4. Main features

Function	Features
Modem	• 3GPP Rel.14 LTE Cat.NB2 • SMS support (Text and PDU) • Real Time Clock
Interfaces	• 2 UARTs (Main with flow control and Auxiliary with RX TX only) • USB 1.1 (debug only) • I2C (as GPIO Alternate function) • 8 GPIOs • Antenna pad

2.5. TX Output Power

Band	Power class
All Bands	Class 3 (23dB)

2.6. Mechanical specifications

2.6.1. Dimensions

The overall dimensions of NL865H2 family are:

- Length: 24.4 mm
- Width: 24.4 mm
- Thickness: 2.25 mm

2.7. Temperature Range

Condition	Range	Note
Operating Temperature Range	-20°C to +55°C	The module is fully functional(*) within this 3GPP temperature range and meets 3GPP specifications.
Extended Temperature Range	-40°C to +85°C	The module is fully functional(*) within this temperature range. The RF Performance may deviate from 3GPP requirements in this extended range. For example: receiver sensitivity or maximum output power may deviate by a few dB due to limitations of physics like higher thermal noise floor at high temperature.
Storage Temperature Range	-40°C to +85°C	-

(*) Functional: if applicable, the module is able to make and receive data calls, send and receive SMS and data traffic.

3. PINS ALLOCATION

Warning:

NL865H2 is adopting a modified 56-pin xL865 Form Factor, pin to pin compatible with the previous 48-pin xL865 FF and with 8 additional pads.

The numbering of the pins has been changed accordingly and attention has to be paid when comparing with previous 48-pin xL865 FF design.

3.1. Pin-out

Pin	Signal	I/O	Function	Type	Comment
Asynchronous Serial Port (USIF0) – Prog. / Data + HW Flow Control					
1	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE	CMOS 1.8V	
2	C125/RING	O	Output for Ring indicator signal (RI) to DTE	CMOS 1.8V	
3	C107/DSR	O	Output for Data set ready signal (DSR) to DTE	CMOS 1.8V	
4	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE	CMOS 1.8V	
5	C105/RTS	I	Input for Request to send signal (RTS) from DTE	CMOS 1.8V	
6	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	CMOS 1.8V	
9	C103/TXD	I	Serial data input (TXD) from DTE	CMOS 1.8V	
10	C104/RXD	O	Serial data output (RXD) to DTE	CMOS 1.8V	
Auxiliary UART					
52	RXD_AUX	I	Auxiliary UART (RX Data)	CMOS 1.8V	
53	TXD_AUX	O	Auxiliary UART (TX Data)	CMOS 1.8V	

USB 1.1 (Debug Port)					
20	USB_D+	I/O	USB differential Data (+)		
19	USB_D-	I/O	USB differential Data (-)		
18	VUSB	I	Power sense for the internal USB transceiver.		Compliant to VUSB from USB V1.1 specification (from 4.4 V to 5.5V)
SIM card interface					
11	SIMVCC	-	External SIM signal – Power supply for the SIM	1.8V	
12	SIMRST	O	External SIM signal – Reset	1.8V	
13	SIMCLK	O	External SIM signal – Clock	1.8V	
14	SIMIO	I/O	External SIM signal – Data I/O	1.8V	
DIGITAL IO					
48	GPIO_01	I/O	Configurable GPIO01	CMOS 1.8	Default is pull-down
47	GPIO_02	I/O	Configurable GPIO02	CMOS 1.8	Default is pull-down
46	GPIO_03	I/O	Configurable GPIO03 Alternate 1: I2C_SDA	CMOS 1.8	Default is pull-down
45	GPIO_04	I/O	Configurable GPIO04 Alternate 1: I2C_SCL	CMOS 1.8	Default is pull-down
33	GPIO_05	I/O	Configurable GPIO05 Alternate 1: I2C_SDA	CMOS 1.8	Default is pull-down
32	GPIO_06	I/O	Configurable GPIO06 Alternate 1: I2C_SCL	CMOS 1.8	Default is pull-down
31	GPIO_07	I/O	Configurable GPIO07 Alternate 1: I2C_SDA	CMOS 1.8	Default is pull-down
30	GPIO_08	I/O	Configurable GPIO08 Alternate 1: I2C_SCL Alternate 2: STAT LED	CMOS 1.8	Default is pull-down

ADC					
15	ADC_IN1	I	Analog To Digital converter Input #1	A/D	10-bit, range 0-1.4V
16	ADC_IN2	I	Analog To Digital converter Input #2	A/D	10-bit, range 0-1.4V
RF Section					
40	MAIN ANTENNA	I/O	Main Antenna (50 ohm)	RF	
Miscellaneous Functions					
7	WAKE*	I	Input Command for PSM Wake Up	CMOS 1.8V	Falling edge trigger
55	RESET*	I	Reset	CMOS 1.8V	Active Low
51	VAUX	O	Supply Output for external accessories / Power ON Monitor	Power	Max10mA
Power Supply					
44	VBATT	I	VBATT	Power	Range: 3.0~3.6 V, recommended value is 3.3V
43	VBATT_PA	I	VBATT_PA	Power	Range: 3.0~3.6 V, recommended value is 3.3V
21	GND	-	Ground	Power	
23	GND	-	Ground	Power	
27	GND	-	Ground	Power	
35	GND	-	Ground	Power	
38	GND	-	Ground	Power	
39	GND	-	Ground	Power	
41	GND	-	Ground	Power	
42	GND	-	Ground	Power	

54	GND	-	Ground	Power
RESERVED				
8	RESERVED	-	RESERVED	
17	RESERVED	-	RESERVED	
22	RESERVED	-	RESERVED	
24	RESERVED	-	RESERVED	
25	RESERVED	-	RESERVED	
26	RESERVED	-	RESERVED	
28	RESERVED	-	RESERVED	
29	RESERVED	-	RESERVED	
36	RESERVED	-	RESERVED	
37	RESERVED	-	RESERVED	
49	RESERVED	-	RESERVED	
50	RESERVED	-	RESERVED	
56	RESERVED	-	RESERVED	

WARNING

Reserved pins must not be connected.

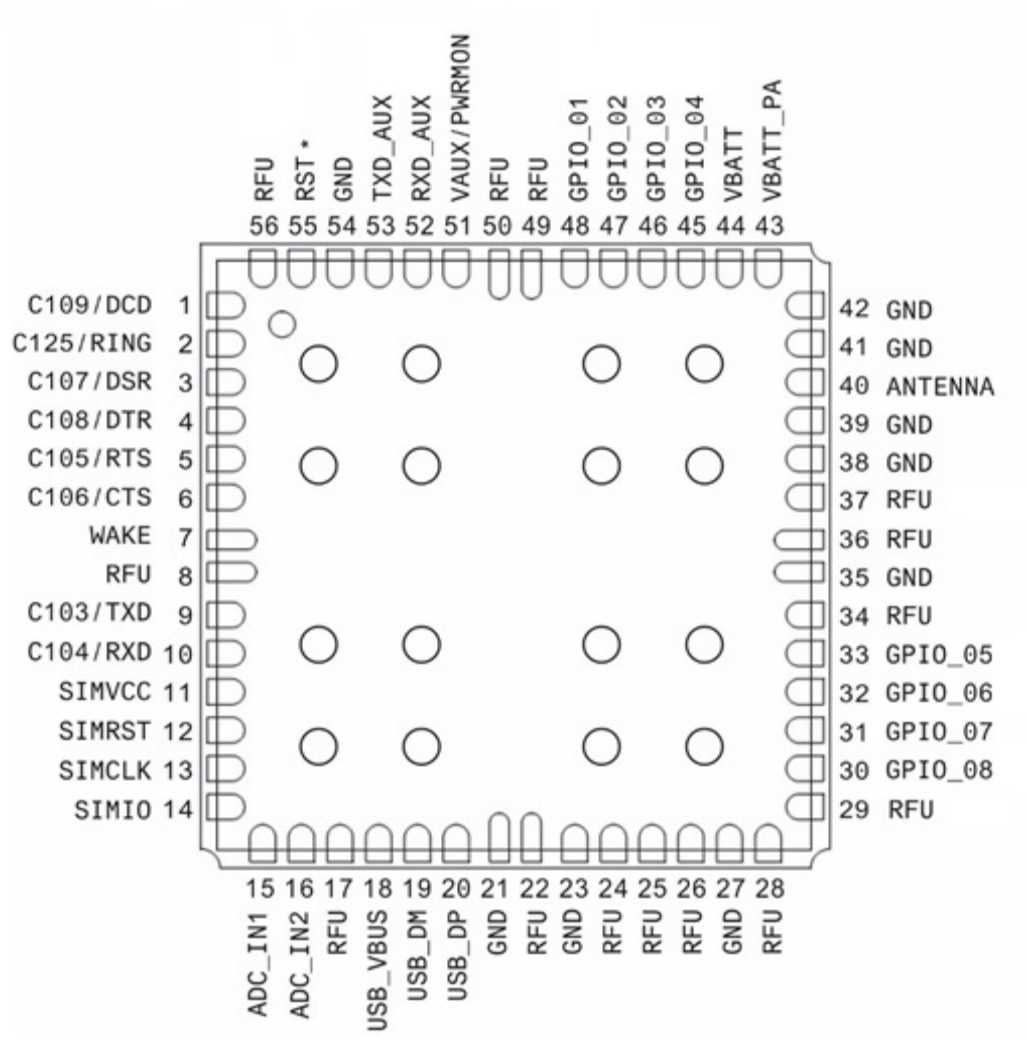
If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

Pad	Signal	Note
44	VBATT	
43	VBATT_PA	
21, 23, 27, 35, 38, 39, 41, 42, 54	GND	
40	MAIN ANTENNA	
9	C103/TXD	
10	C104/RXD	
5	C105/RTS	
6	C106/CTS	
11	SIMVCC	
12	SIMRST	
13	SIMCLK	
14	SIMIO	
7	WAKE*	
55	RESET*	
51	VAUX	
20	USB_D+	On TP or a Connector
19	USB_D-	On TP or a Connector
18	VUSB	On TP or a Connector

RTS pin should be connected to the GND (on the module side) if flow control is not used. The above pins are also necessary to debug the application when the module is assembled on it so we recommend connecting them also to dedicated test point.

3.2. LGA Pads Layout

TOP VIEW



4. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

4.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfil the following requirements:

Power Supply	Value
Nominal Supply Voltage	3.3V
Operating Voltage Range	3.00 V÷ 3.60 V
Extended Voltage Range	2.10 V÷ 3.63 V
$VBAT_{min}$	2.10V
Absolute Maximum Voltage	3.63V

NOTE:

The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded.

The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 500mA.

4.2. Operating Modes

This module has three operating modes, which can determine availability of functions for different levels of power-saving.

Mode	Function
Active	In active mode, all functions of the module are available and all processors are active. Data transmission and reception can be performed. Transitions to idle or PSM mode can be initiated in active mode.
Idle	In idle mode, the module is in light sleep and network connection is maintained (module in DRX/eDRX mode); paging messages can be received; transitions to active mode or PSM can be initiated in idle mode.
PSM	In PSM, the module is in deeper sleep and only the 32kHz RTC is working. The network is disconnected, and paging messages cannot be received either. When MO (Mobile Originated) data are sent or the periodic TAU (Tracking Area Update) timer T3412 expires, or when WAKE* drop edge trigger, the module will be woken up.

4.3. Power Consumption

The table below shows the operating power consumption of the NL865H2-W1 in different operating modes.

Status	Description	Average	Max. value	Unit
AT+CFUN=0	Turn off radio and SIM power	6		mA
PSM mode	Power Save Mode	4.238		uA
IDLE	Idle mode	547		uA
Operating current under NB-IoT mode	Band1, Pout=23dBm	133	212	mA
	Band2, Pout=23dBm	127	200	mA
	Band3, Pout=23dBm	115	186	mA
	Band4, Pout=23dBm	115	182	mA
	Band5, Pout=23dBm	108	175	mA
	Band8, Pout=23dBm	119	193	mA
	Band12, Pout=23dBm	110	182	mA
	Band13, Pout=23dBm	106	172	mA
	Band17, Pout=23dBm	112	179	mA
	Band18, Pout=23dBm	118	188	mA
	Band19, Pout=23dBm	117	186	mA
	Band20, Pout=23dBm	119	192	mA
	Band25, Pout=23dBm	122	196	mA
	Band26, Pout=23dBm	119	187	mA
	Band28, Pout=23dBm	117	187	mA

	Band66, Pout=23dBm	116	183	mA
	Band71, Pout=23dBm	129	210	mA
	Band85, Pout=23dBm	113	184	mA

4.4. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

4.4.1. Electrical Design Guidelines

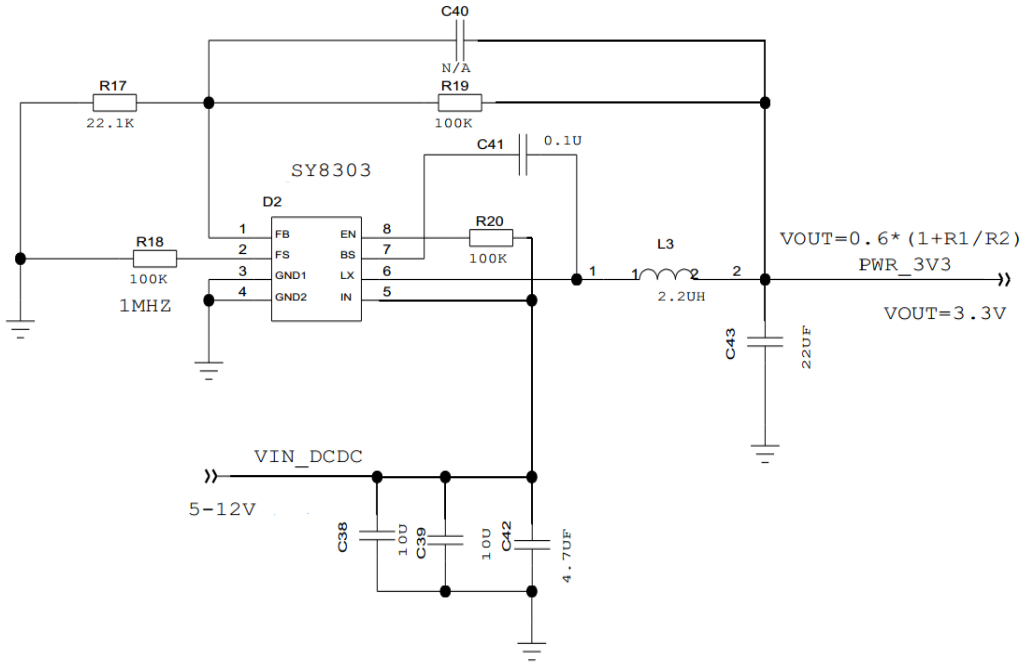
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.4.1.1. +5V/+12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.3V, hence due to the difference between the input source and the desired output, a switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the module from power polarity inversion. This can be the same diode as for spike protection.

The reference circuit is as follow:



4.4.1.2. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.3V and the maximum voltage allowed is 3.63V.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the NL865H2-W1 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.

WARNING:

The three cells Ni/Cd or Ni/MH 3.6 V Nom. Battery types or 4V PB types MUST NOT BE USED DIRECTLY since their maximum voltage can rise over the absolute maximum voltage for the NL865H2-W1 and damage it.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with NL865H2-W1. Their use can lead to overvoltage on the NL865H2-W1 and damage it. USE ONLY Li-Ion battery types.

4.4.2. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done considering the values described in the “Power Consumption” chapter.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

For the heat generated by the module, you can consider it to be during transmission 0.99W max during Data call.

This generated heat will be mostly conducted to the ground plane under the module; you must ensure that your application can dissipate it.

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

4.4.3. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The Bypass low ESR capacitor must be placed close to the Telit NL865H2-W1 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the NL865H2-W1 is wide enough to ensure a dropless connection even during the 500mA current peaks.

- The protection diode must be placed close to the input connector where the power source is drained.

- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually)

- The use of a good common ground plane is suggested.

- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.

- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.

- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.

- A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

4.5. RTC Bypass out

The NL865H2-W1 module is provided by an internal RTC section but its reference supply is VBATT.So, in order to maintain active the RTC programming, VBATT should not be removed.

4.6. VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module. The signal is in common with the PWRMON (module powered ON indication) function. This output is always active when the module is powered ON. The operating range characteristics of the supply are:

Item	Min	Typical	Max
Output voltage	1.62V	1.80V	1.98V
Output current	-	-	10mA
Output bypass capacitor		0.1uF	

NOTE:
The Output Current MUST never be exceeded; care must be taken when designing the application section to avoid having an excessive current consumption.
If the Current is exceeding the limits it could cause a Power Off of the module.

NOTE:
VAUX max output current is shared with the other GPIOs for a maximum load of 10mA.

Warning:
The current consumption from VAUX/PWRMON increases the modem temperature.

5. DIGITAL SECTION

5.1. Logic Levels

ABSOLUTE MAXIMUM RATINGS:

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.1V

OPERATING RANGE – INTERFACE LEVELS (1.8V CMOS):

Parameter	Min	Max
Input high level	1.35V	1.98V
Input low level	-0.3V	0.63V
Output high level	1.35 V	1.98V
Output low level	0	0.45

CURRENT CHARACTERISTICS:

Parameter	MAX	Description
Input Current	5uA	Digital high input,pull-down disable
	5uA	Digital low input,pull-up disable

5.2. Power On

The NL865H2-W1 module is automatically powering on itself when supplied.

NOTE:

To check if the device has powered on, the hardware line VAUX/PWRMON should be monitored.

The power-off duration is required to be at least 5s before the module is powered on.

5.3. Unconditional Restart

To unconditionally restart the NL865H2-W1, the pad RESET* must be tied low for at least 400 milliseconds and then released.
The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stuck waiting for some network or SIM responses.
The unconditional hardware restart must always be implemented on the boards and the software must use it as an emergency exit procedure.

5.3.1. PIN DESCRIPTION

Signal	Function	I/O	Pad
RESET*	Unconditional Reset of the Module	I	55

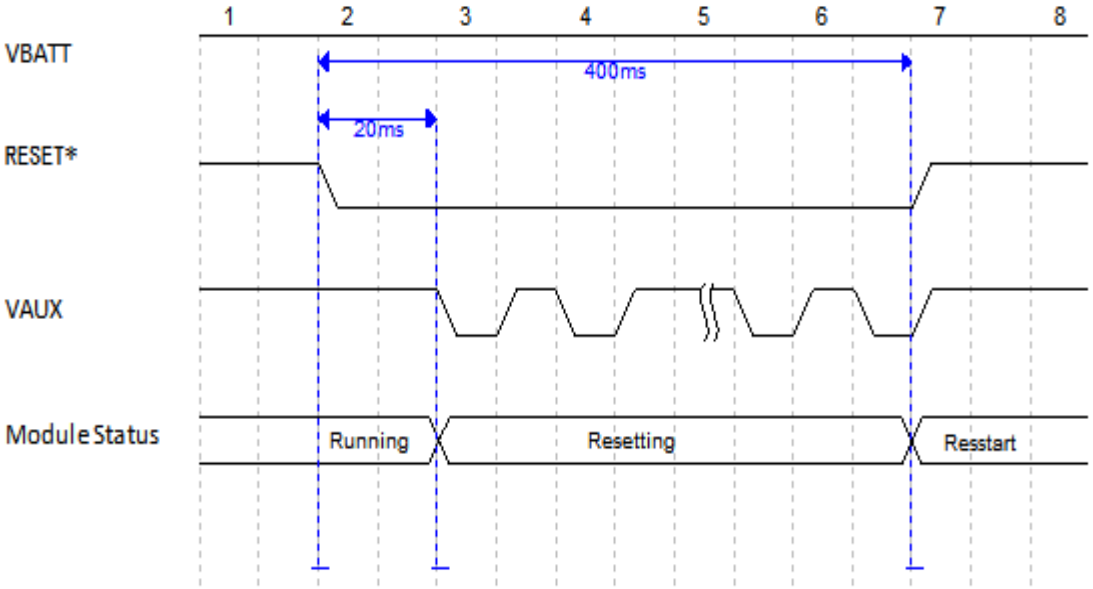
There are two way to reset the module you can choose:

1：Through AT command of “AT+TRST”

2：Reset the module through RST pin

When the software stops response, you can pulled down RST 400ms to reset the module's system.

The RST timing is shown in the following figure below:



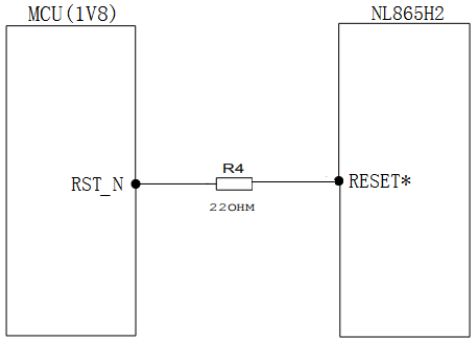
5.3.2. Operating levels

The RESET* line is connected to VBATT with a Pull Up so the electrical levels on this pin are aligned to the main supply level.

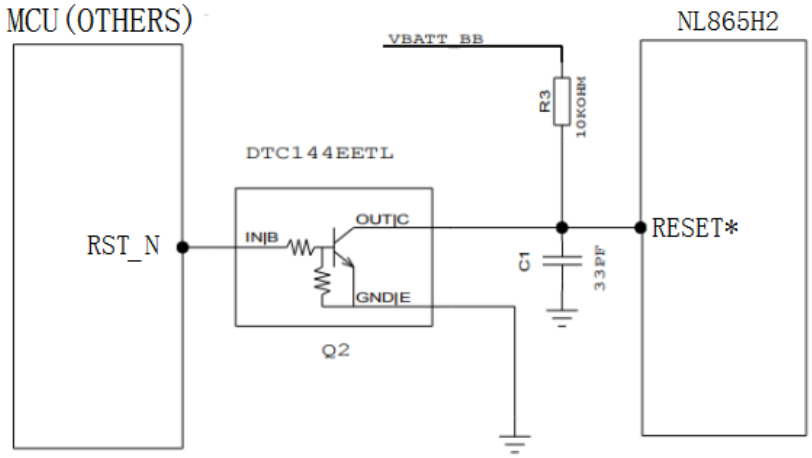
WARNING:

The hardware unconditional Reset must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure.

The RST circuit design is divided into two types:1.8V and non-1.8V. The 1.8V RST reference circuit design is shown below. The resistor value is for reference only. Please fine tune according to the specific application:



The non-1.8V RST reference circuit design is shown below.



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NE865H2 when the module is powered off or during a reboot transition.

NOTE:

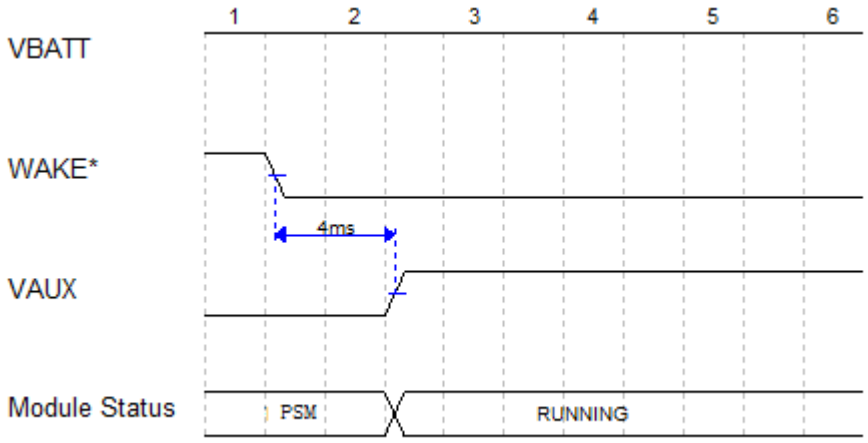
To proper power on again the module please refer to the related paragraph (“Power ON”)

The unconditional hardware reboot must always be implemented on the boards and should be used only as an emergency exit procedure.

5.1. WAKEUP from PSM

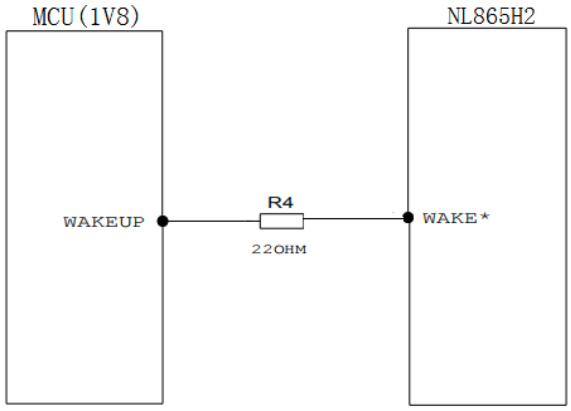
5.1.1. Pin Description

The module is provided by an input line named WAKE* used to wakeup the module from the deep power saving state (PSM). The signal is active LOW.
The following figure is the signal waveform:

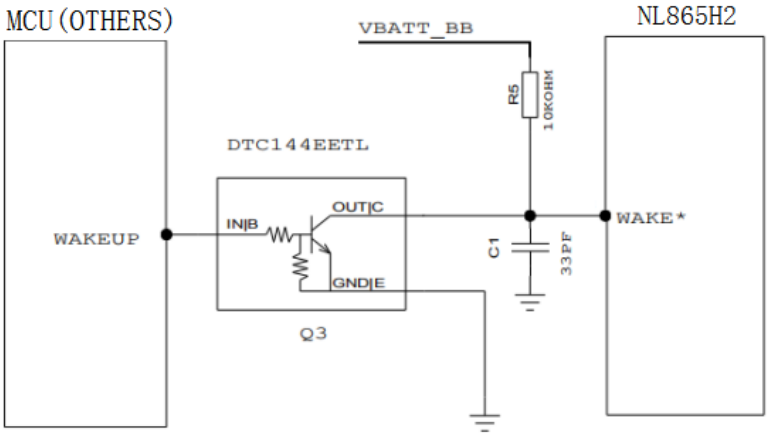


5.1.2. Application Example

The WAKEUP circuit design is divided into two types:1.8V and non-1.8V. The 1.8V WAKEUP reference circuit design is shown below. The resistance value is for reference only. Please fine tune according to the specific customer's application:



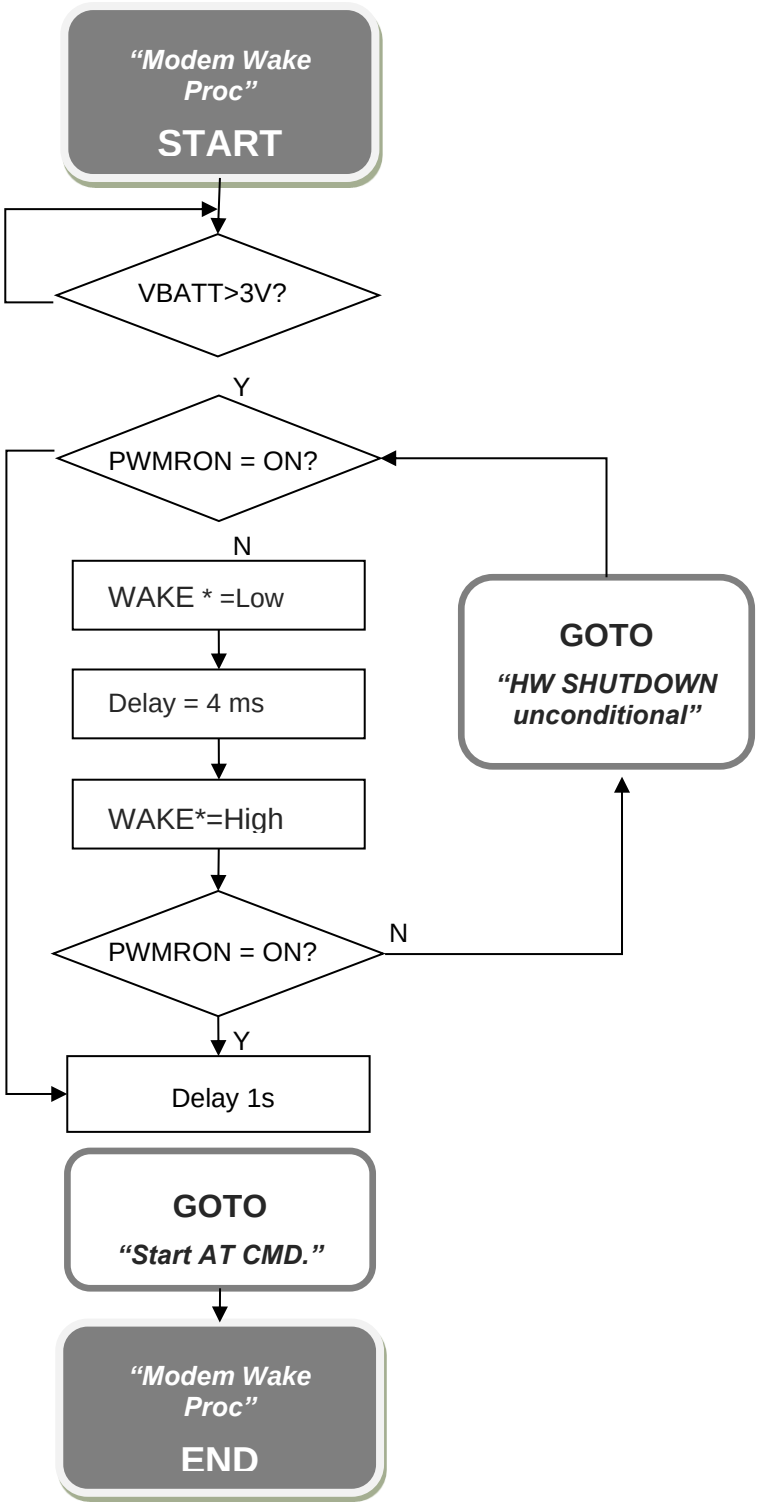
When the WAKEUP on the MCU side is 3.3V or other level domain, the reference circuit design is shown below.



The resistor and capacitance in Figure are only the recommended value and they need to be tuned according to the specific customer's application.

After the module is woken up by the WAKEUP key, it will sleep again after 5 seconds without doing other services.

The following flowchart is describing the WAKE procedure:



5.2. Communication ports

The NL865H2-W1 module is provided with by 2 Asynchronous serial ports:

- MODEM SERIAL PORT 1 (Main)
- MODEM SERIAL PORT 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. On the NL865H2-W1 the ports are CMOS 1.8.

5.2.1.1. Modem serial port 1

The serial port 1 on the NL865H2-W1 is a +1.8V UART . It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. The following table is listing the available signals:

RS232 Pin	Signal	NL865H2 PAD	Name	Usage
1	C109/DCD	**1**	Data Carrier Detect	Output from the NL865H2 that indicates the carrier presence
2	C104/RXD	**10**	Transmit line *see Note	Output transmit line of NL865H2 UART
3	C103/TXD	**9**	Receive line *see Note	Input receive of the NL865H2 UART
4	C108/DTR	**4**	Data Terminal Ready	Input to the NL865H2 that controls the DTE READY condition
6	C107/DSR	**3**	Data Set Ready	Output from the NL865H2 that indicates the module is ready
7	C106/CTS	**5**	Clear to Send	Output from the NL865H2 that controls the Hardware flow control
8	C105/RTS	**6**	Request to Send	Input to the NL865H2 that controls the Hardware flow control
9	C125/RING	**2**	Ring Indicator	Output from the NL865H2 that indicates the incoming call condition

NOTE:
According to V.24, some signal names are referred to the application side, therefore on the NL865H2 side these signal are on the opposite direction:
TXD on the application side will be connected to the receive line (here named C103/TXD)
RXD on the application side will be connected to the transmit line (here named C104/RXD)

For a minimum implementation, only the TXD, RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NL865H2 when the module is powered off or during an ON/OFF transition.

5.2.1.2. Modem serial port 2

The secondary serial port on the NL865H2 is a CMOS1.8V with only the RX and TX signals. The signals of the NL865H2 serial port are:

PAD	Signal	I/O	Function	Type	NOTE
53	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 1.8V	
52	RX_AUX	I	Auxiliary UART (RX Data from DTE)	CMOS 1.8V	

NOTE:
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NL865H2 when the module is powered off or during an ON/OFF transition.

Refer to NL865H2 series AT command reference guide for port configuration.

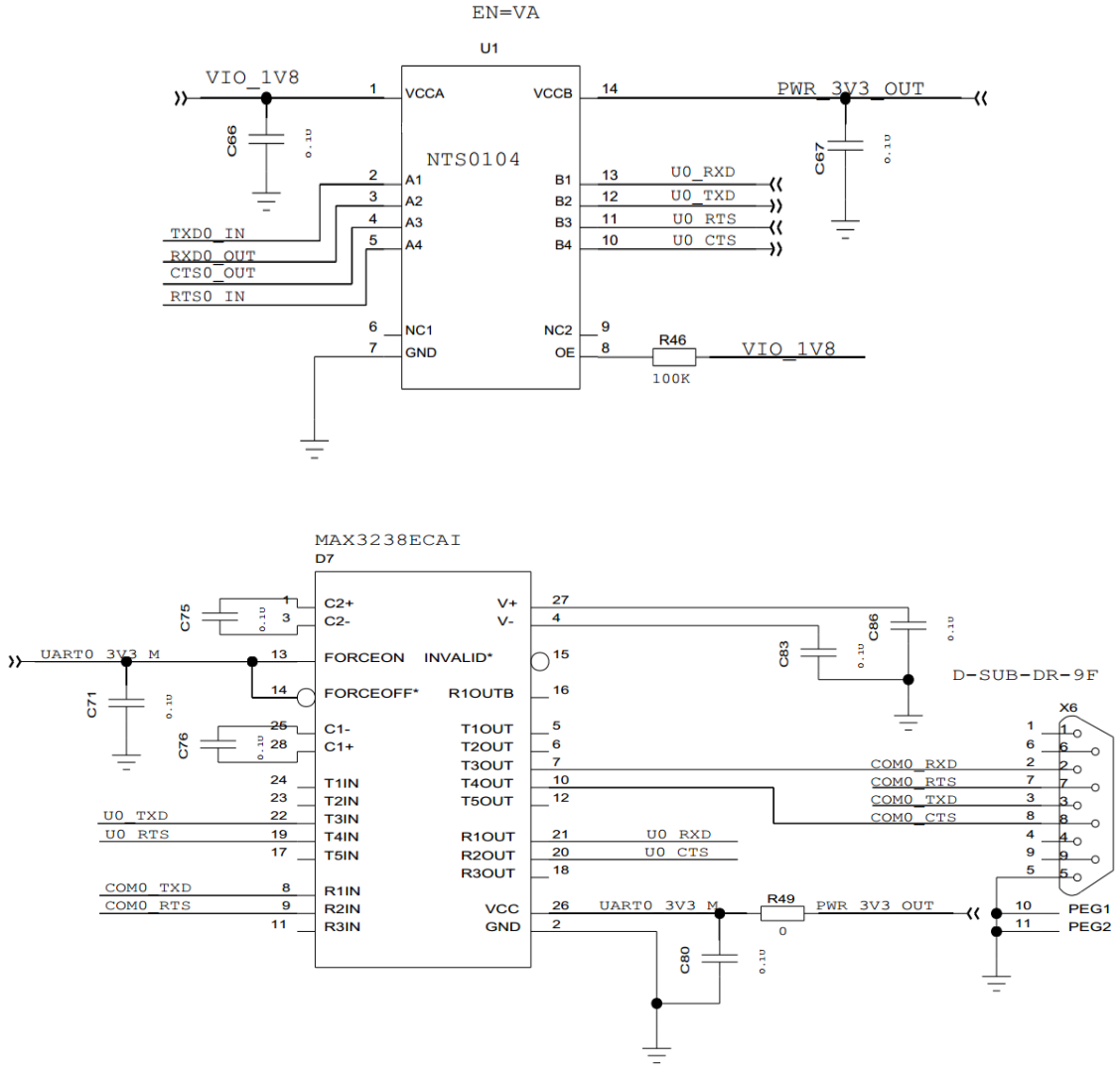
5.2.1.3. RS232 LEVEL TRANSLATION

In order to interface the module with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

- invert the electrical signal in both directions;
- change the level from 0/1.8V to +15/-15V .

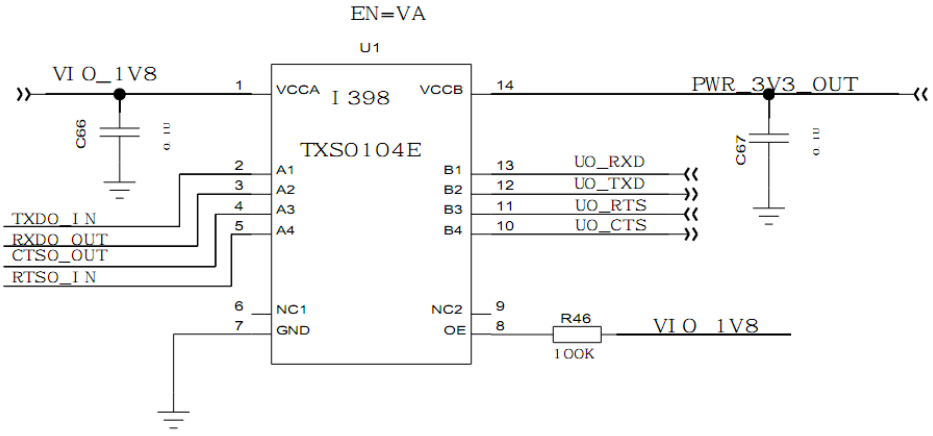
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

An example of level translation circuitry of this kind is:



The example is done with a MAXIM MAX3238 Transceiver that could accept supply voltages of 3.3V DC.

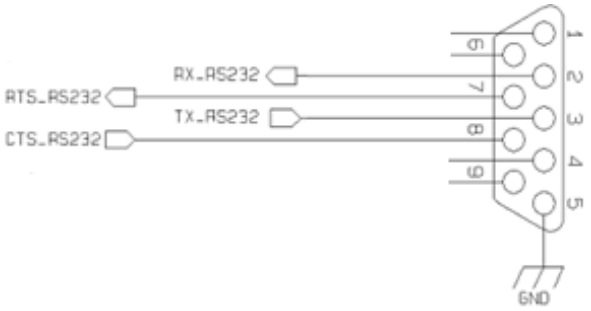
Second solution could be done using a MAXIM transceiver TXS0104E. In this case, there is no need to use a single chip level translator:



NOTE:

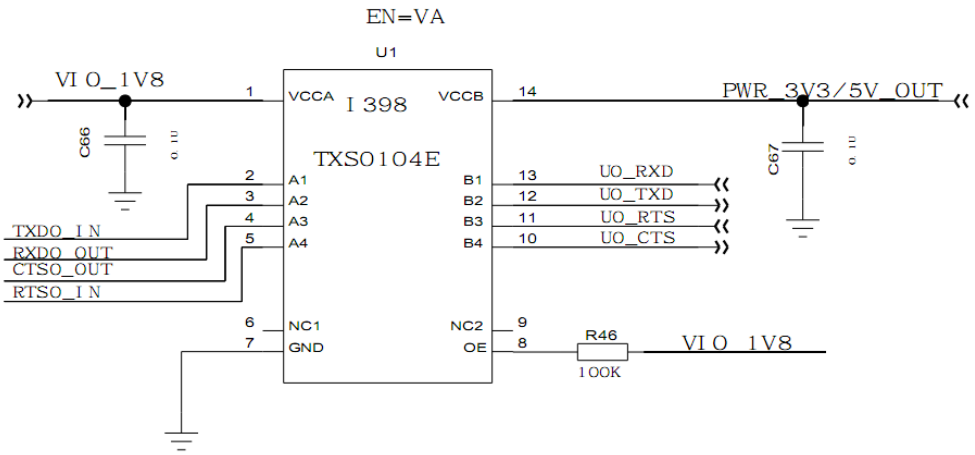
In this case has to be taken in account the length of the lines on the application to avoid problems in case of High-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



5.2.2. 3.3V/5V UART level translation

If the customer's application uses a microcontroller with a serial port (UART) that works at a voltage different from 1.8V, then a circuitry has to be provided to adapt the different levels of the two set of signals. As for the RS232 translation there are a multitude of single chip translators. For example a possible translator circuit for a 5V/3.3V TRANSMITTER / RECEIVER can be:



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when the module is powered OFF or during an ON/OFF transition.

5.3. General purpose I/O

The NL865H2-W1 module is provided by a set of Configurable Digital Input / Output pins (CMOS 1.8)

Input pads can only be read; they report the digital value (high or low) present on the pad at the read time. Output pads can only be written or queried and set the value of the pad output. An alternate function pad is internally controlled by the NL865H2-W1 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the NL865H2-W1:

PAD	Signal	I/O	Default State	Note
48	GPIO_01	I/O	Input , Pull-down	Configurable GPIO01
47	GPIO_02	I/O	Input , Pull-down	Configurable GPIO02
46	GPIO_03	I/O	Input , Pull-down	Configurable GPIO03 Alternate 1: I2C_SDA
45	GPIO_04	I/O	Input , Pull-down	Configurable GPIO04 Alternate 1: I2C_SCL
33	GPIO_05	I/O	Input , Pull-down	Configurable GPIO05 Alternate 1: I2C_SDA
32	GPIO_06	I/O	Input , Pull-down	Configurable GPIO06 Alternate 1: I2C_SCL
31	GPIO_07	I/O	Input , Pull-down	Configurable GPIO07 Alternate 1: I2C_SDA
30	GPIO_08	I/O	Input , Pull-down	Configurable GPIO08 Alternate 1: I2C_SCL Alternate 2: STAT LED

WARNING:

During power up the GPIOs may be subject to transient glitches.

NOTE:
The internal GPIO's pull up/pull down could be set to the preferred status for the application using the AT#GPIO command.
Please refer for the AT Commands User Guide for the detailed command Syntax.

5.3.1. Using a GPIO as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO. If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to VAUX.

NOTE:
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the NL865H2-W1 when the module is powered off or during a reboot transition.
The VAUX pin can be used for input pull up reference or/and for ON monitoring.

5.3.2. Using a GPIO as OUTPUT

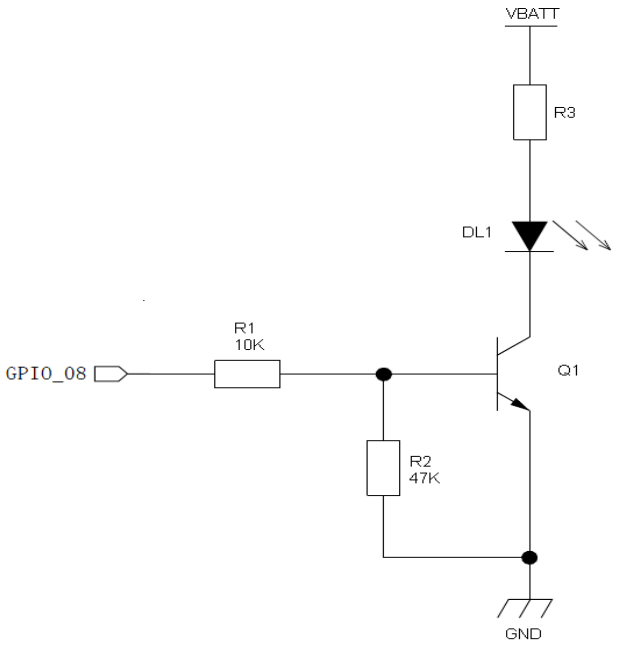
The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

5.3.3. Indication of network service availability

The STAT LED status shows information on the network service availability and Call status. In the NL865H2-W1 modules, the STAT LED needs an external transistor to drive an external LED. Therefore, the status indicated in the following table is reversed with respect to the pin status.
The STAT LED is available as Alternate function of GPIO_08.

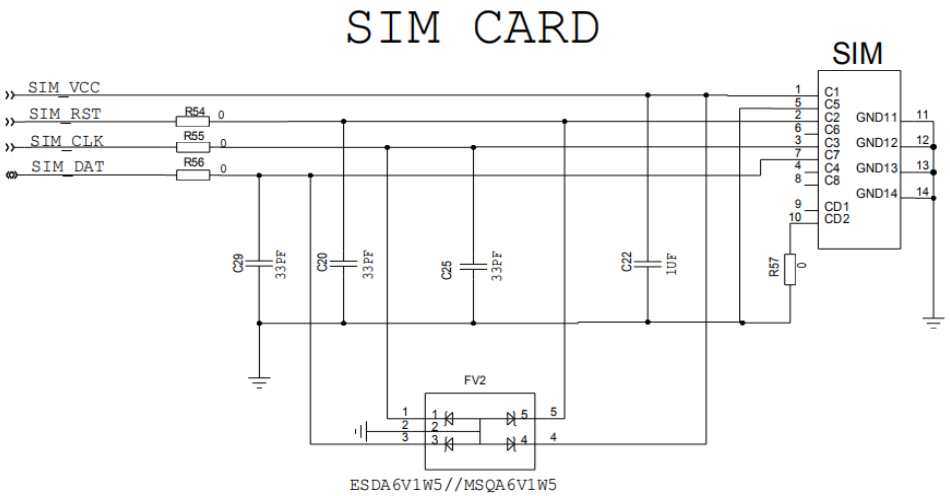
Device Status	Led Status
Device off	Permanently off
Offline	Frequency 1Hz, Duty cycle 50%
Online	Frequency 0.3Hz, Duty cycle 10%
Data Sending	Frequency 10Hz, Duty cycle 50%

A schematic example could be:



5.4. External SIM Holder

SIM circuit reference design is as follows. The minimum value of Capacitor on SIMVCC is 1uF.



5.5. ADC Converter

The NL865H2-W1 is provided by two AD converters. They are able to read a voltage level in the range of 0÷1.4 volts applied on the ADC pin input, store and convert it into 10 bit word. The input lines are named as **ADC_IN1** and **ADC_IN2.**

The following table is showing the ADC characteristics:

Item	Min	Typical	Max	Unit
Input Voltage range	0	-	1.4	Volt
AD conversion	-	-	10	bits
Input Resistance	33	-	-	Mohm
Input Capacitance	-	0.1	-	pF

Refer to AT Commands Reference Guide for the full description of the commands to control the ADC.

6. RF SECTION

6.1. Antenna requirements

6.1.1. Main Antenna

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit NL865H2-W1 device shall fulfil the following requirements:

Item	Value
Frequency range	NB-IOT B1, B2, B3, B4, B5, B8, B12, B13, B17, B18, B19, B20, B25,B26, B28, B66, B71, B85
Gain	>0dBi
Impedance	50 Ohm
Input power	>24dBm average power
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfil all regulatory requirements)

6.1.2. PCB Design guidelines

When using the NL865H2-W1, since there's no antenna connector on the module, the antenna must be connected to the NL865H2-W1 antenna pad by means of a transmission line implemented on the PCB.
In the case the antenna is not directly connected at the antenna pad of the NL865H2-W1, then a PCB line is needed in order to connect with it or with its connector.
This transmission line shall fulfil the following requirements:

Item	Value
Characteristic Impedance	50 ohm
Max Attenuation	0,3 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	Cold End (Ground Plane) of antenna shall be equipotential to the NL865H2-W1 ground pins

The transmission line should be designed according to the following guidelines:

- Ensure that the antenna line impedance is 50 ohm;
- Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0,3 dB;
- Antenna line must have uniform characteristics, constant cross section; avoid meanders and abrupt curves;
- Keep, if possible, one layer of the PCB used only for the Ground plane;
- Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias every 2mm at least;
- Place EM noisy devices as far as possible from NL865H2-W1 antenna line;
- Keep the antenna line far away from the NL865H2-W1 power supply lines;
- If you have EM noisy devices around the PCB hosting the NL865H2-W1, such as fast switching Ics, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.

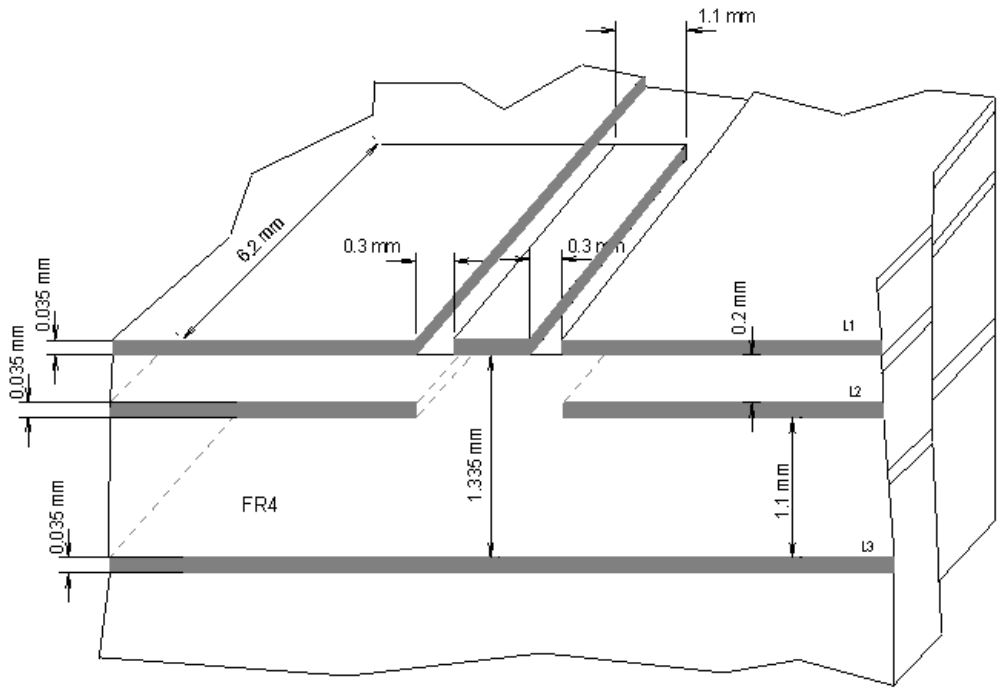
- If you don't have EM noisy devices around the PCB of NL865H2-W1, by using a micro strip on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;

6.1.2.1. Transmission line design

During the design of the NL865H2-W1 interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity $\varepsilon_r = 4.6 \pm 0.4$ @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

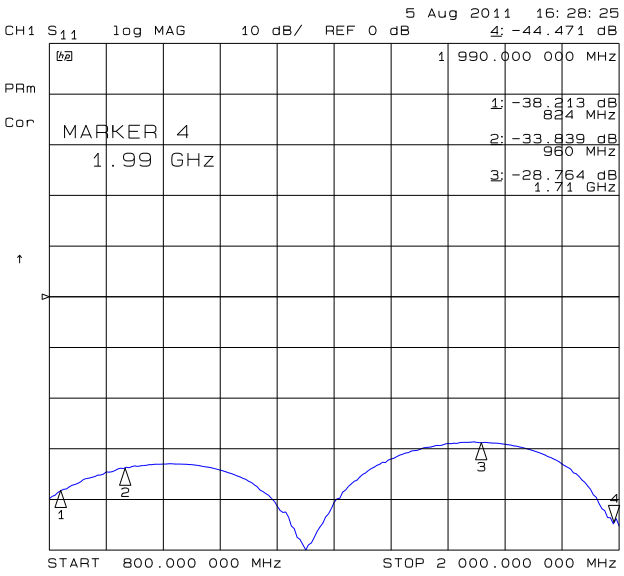
A characteristic impedance of nearly 50 Ω is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:



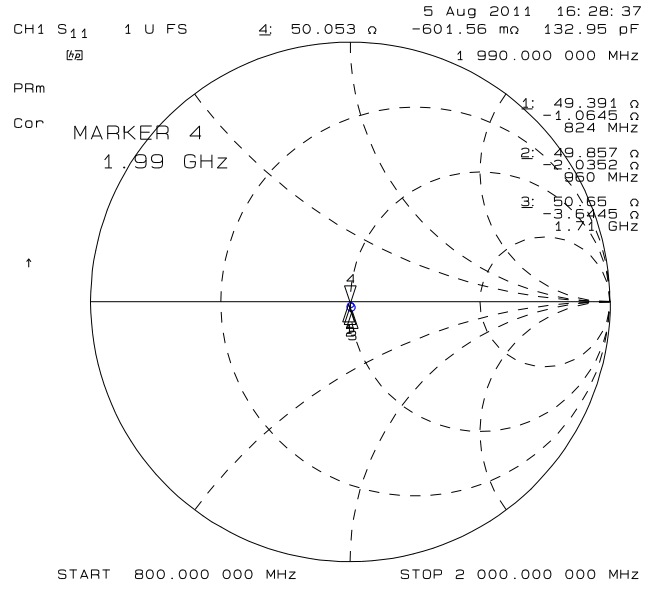
6.1.2.2. Transmission Line Measurements

An HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.

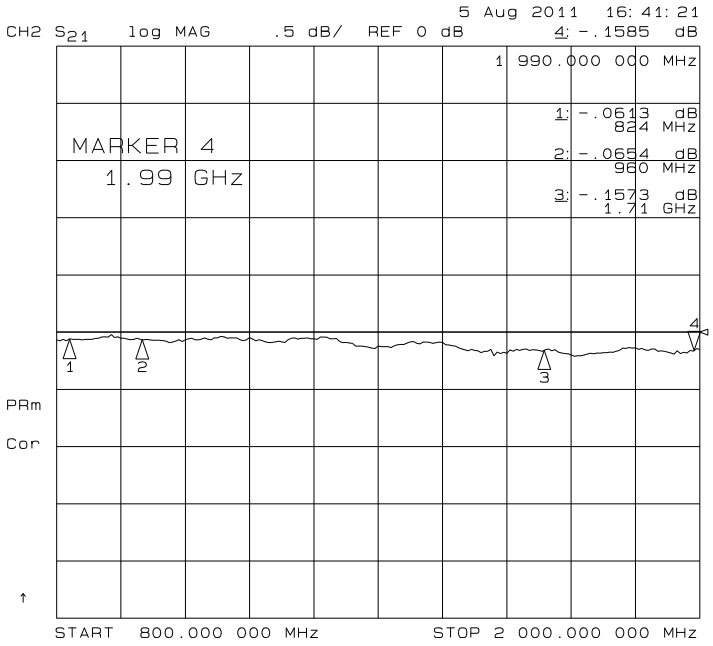
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:



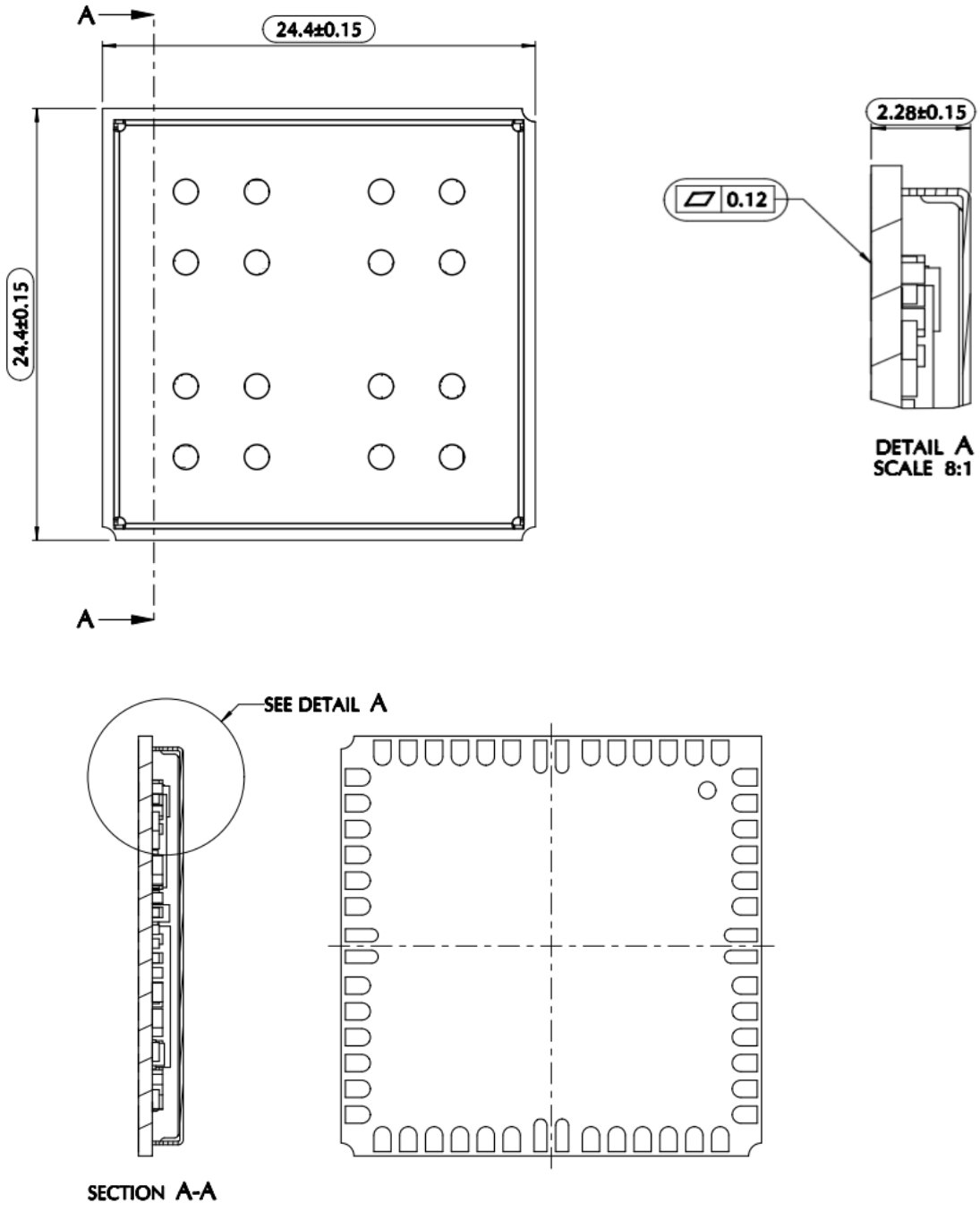
Insertion Loss of G-CPW line plus SMA connector is shown below:



6.1.2.3. Antenna Installation Guidelines

- Install the antenna in a place covered by the LTE signal.
- The Antenna must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter;
- Antenna shall not be installed inside metal cases
- Antenna shall be installed also according Antenna manufacturer instructions.

7. MECHANICAL DESIGN



NOTE:

Dimensions in mm.

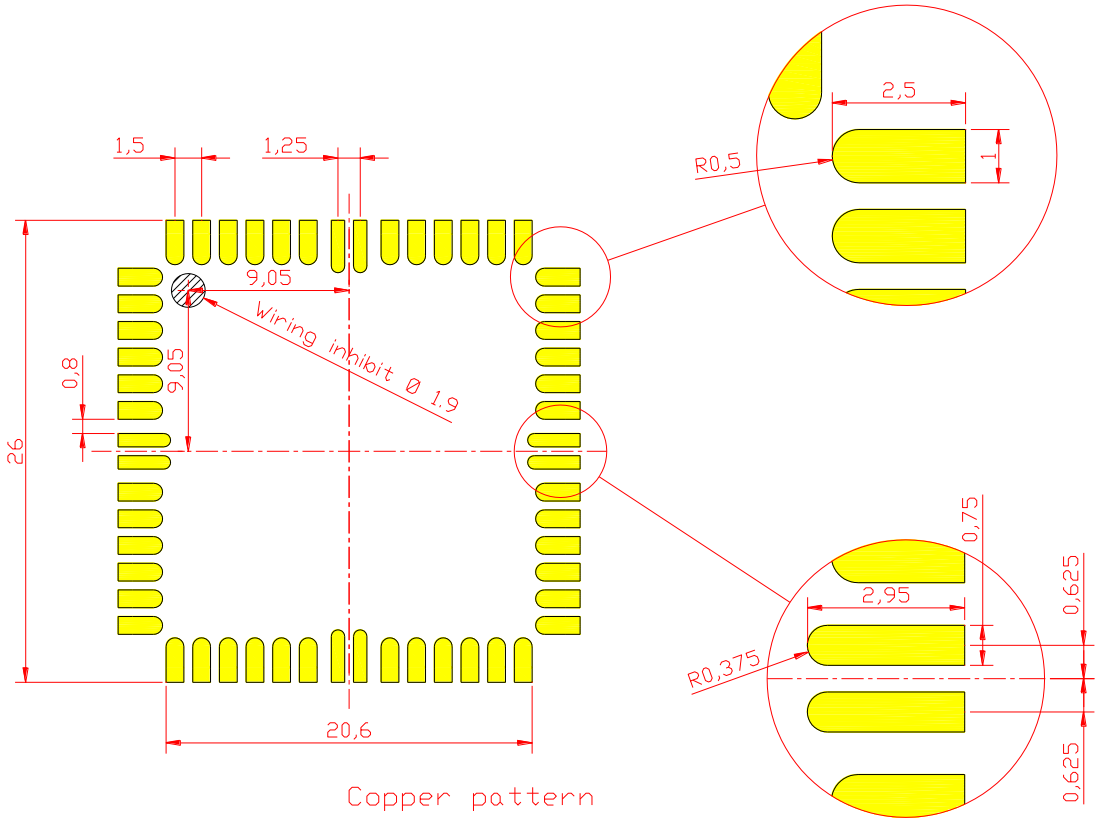
General Tolerance ±0.15mm, The tolerance is not cumulative.

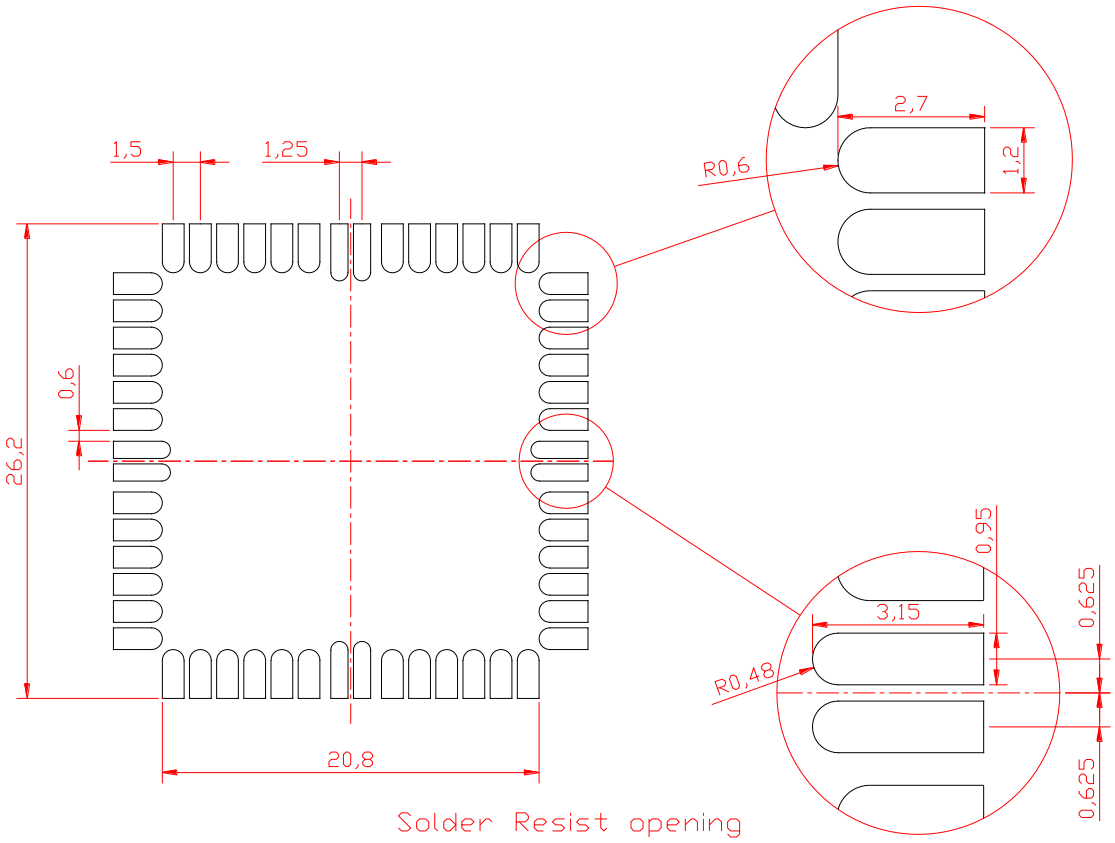
8. APPLICATION PCB DESIGN

8.1. General

The NL865H2 modules have been designed to be compliant with a standard lead-free SMT process.

8.2. Footprint





In order to easily rework the NL865H2 is suggested to consider on the application a 1.5 mm placement inhibit area around the module.

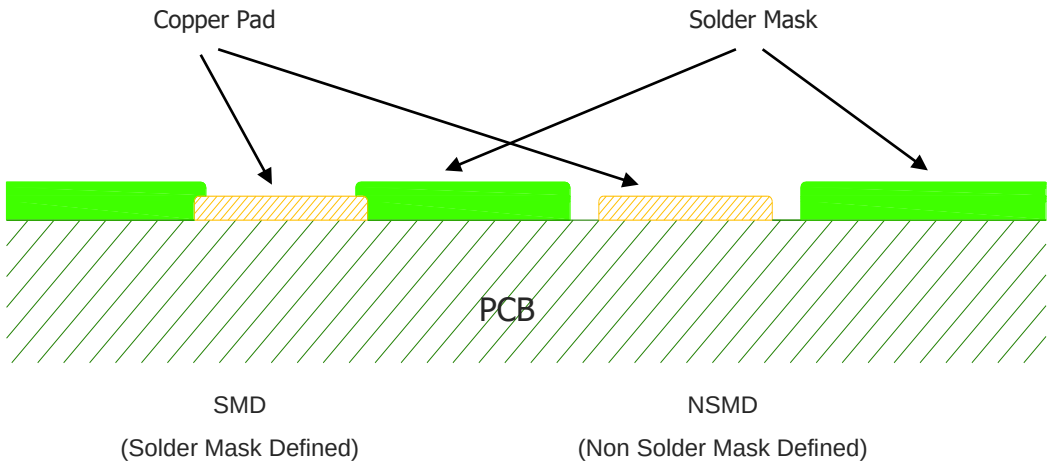
It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

NOTE:

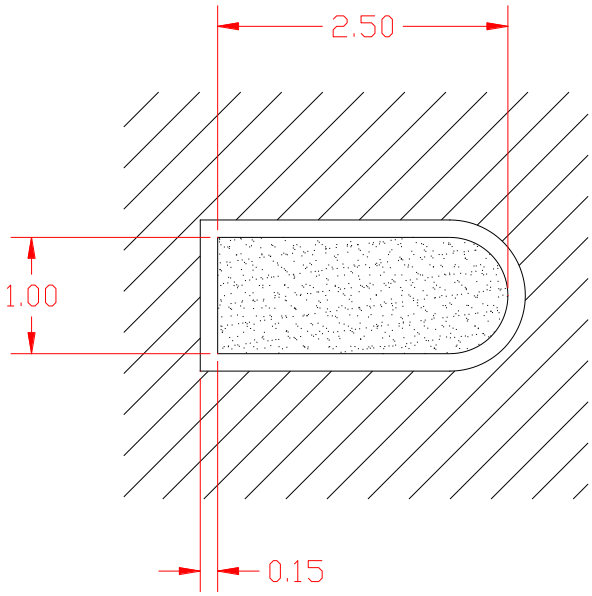
In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

8.3. PCB pad design

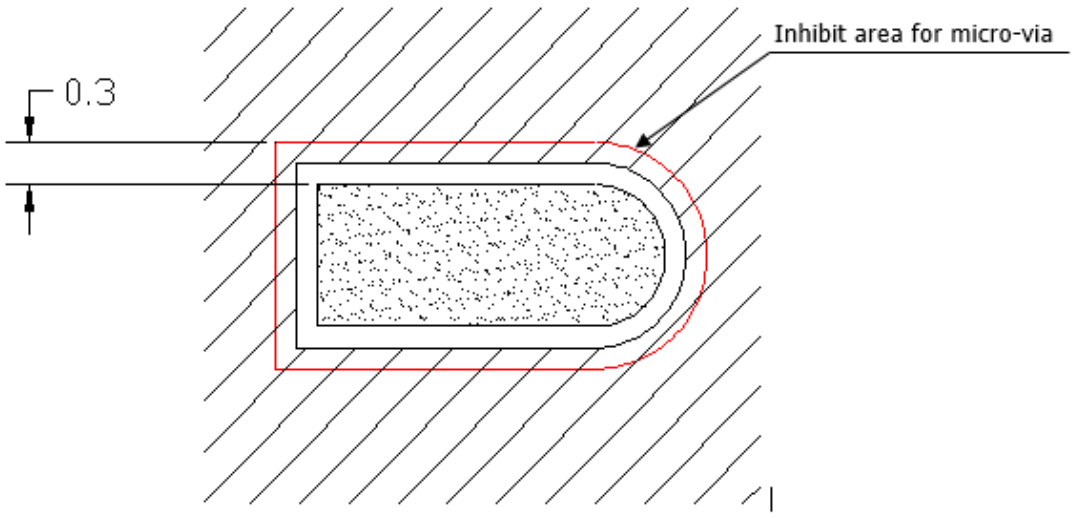
Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



8.4. PCB pad dimensions



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).



Holes in pad are allowed only for blind holes and not for through holes.
Recommendations for PCB pad surfaces:

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.03 – 0.15	good solder ability protection

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.
It is not necessary to panel the application PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

8.5. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

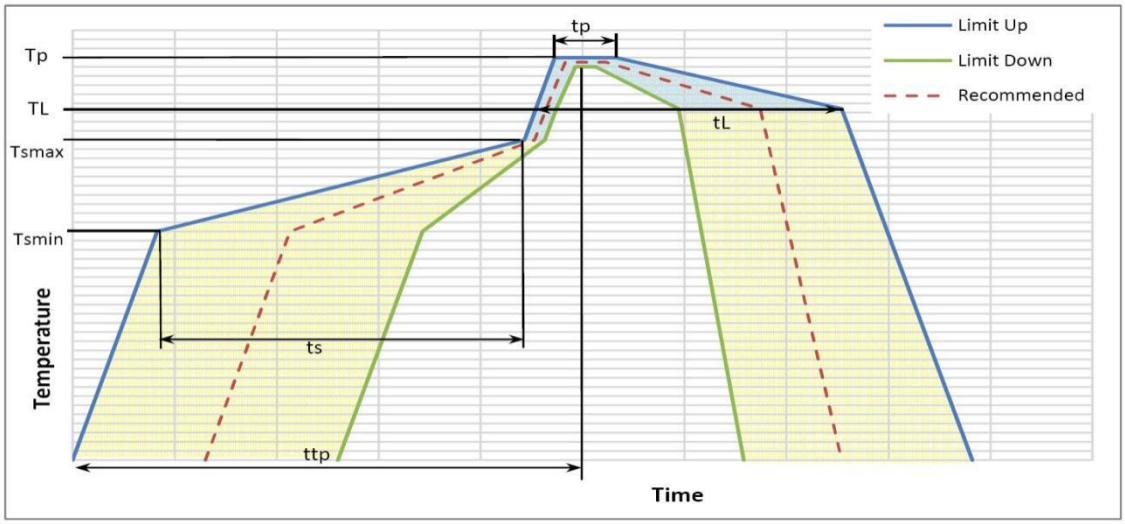
8.6. Solder paste

Item	Lead Free
Solder Paste	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

8.7. Solder Reflow

Recommended solder reflow profile:



Warning:

The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat **– Temperature Min (Tsmin)** **– Temperature Max (Tsmax)** **– Time (min to max) (ts)**	 150°C 200°C 60-180 seconds
Tsmax to TL **– Ramp-up Rate**	 3°C/second max
Time maintained above: **– Temperature (TL)** **– Time (tL)**	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

NOTE:
All temperatures refer to topside of the package, measured on the package body surface

WARNING:
THE NL865H2-W1 MODULE WITHSTANDS ONE REFLOW PROCESS ONLY.

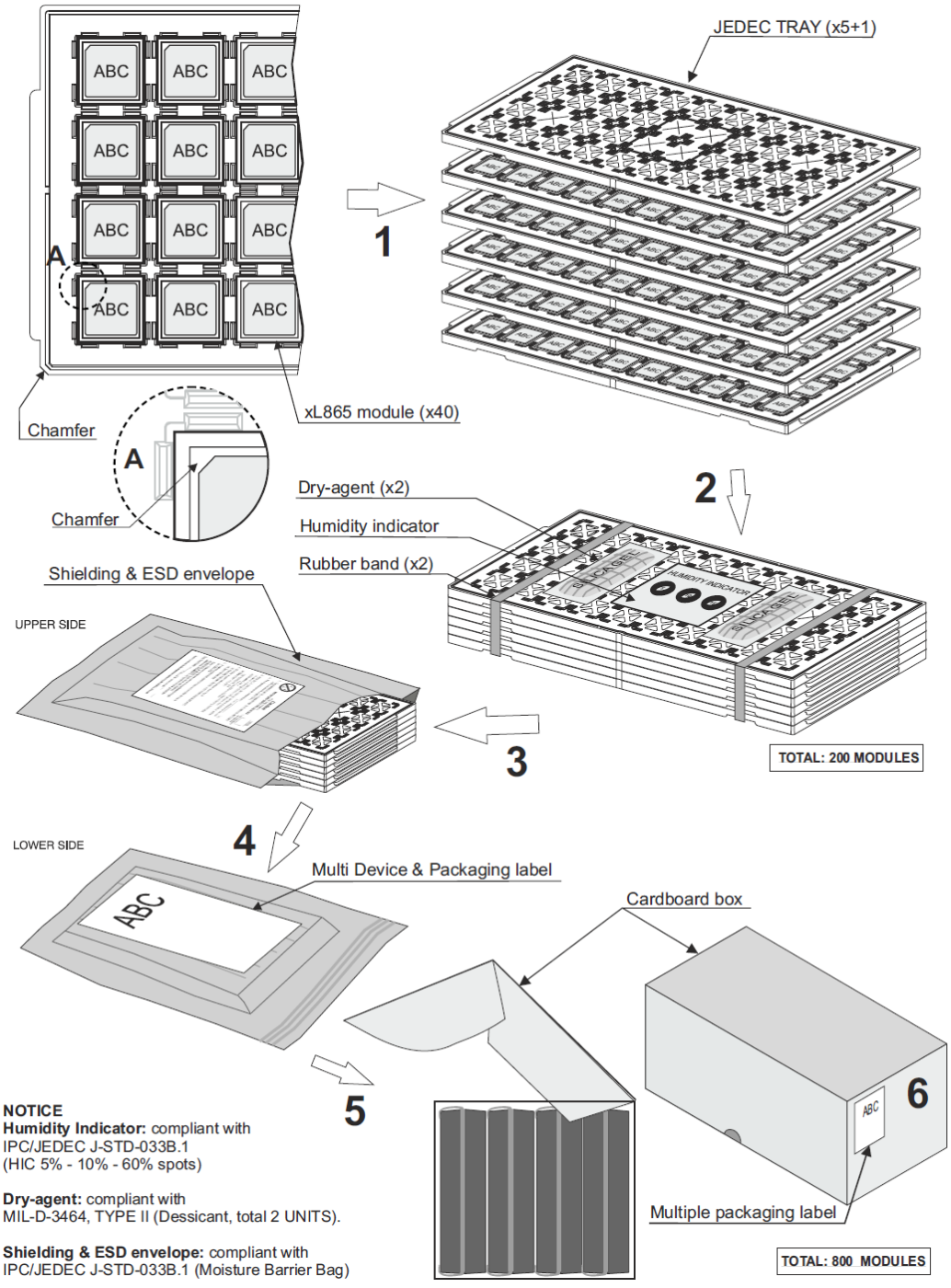
9. PACKAGING

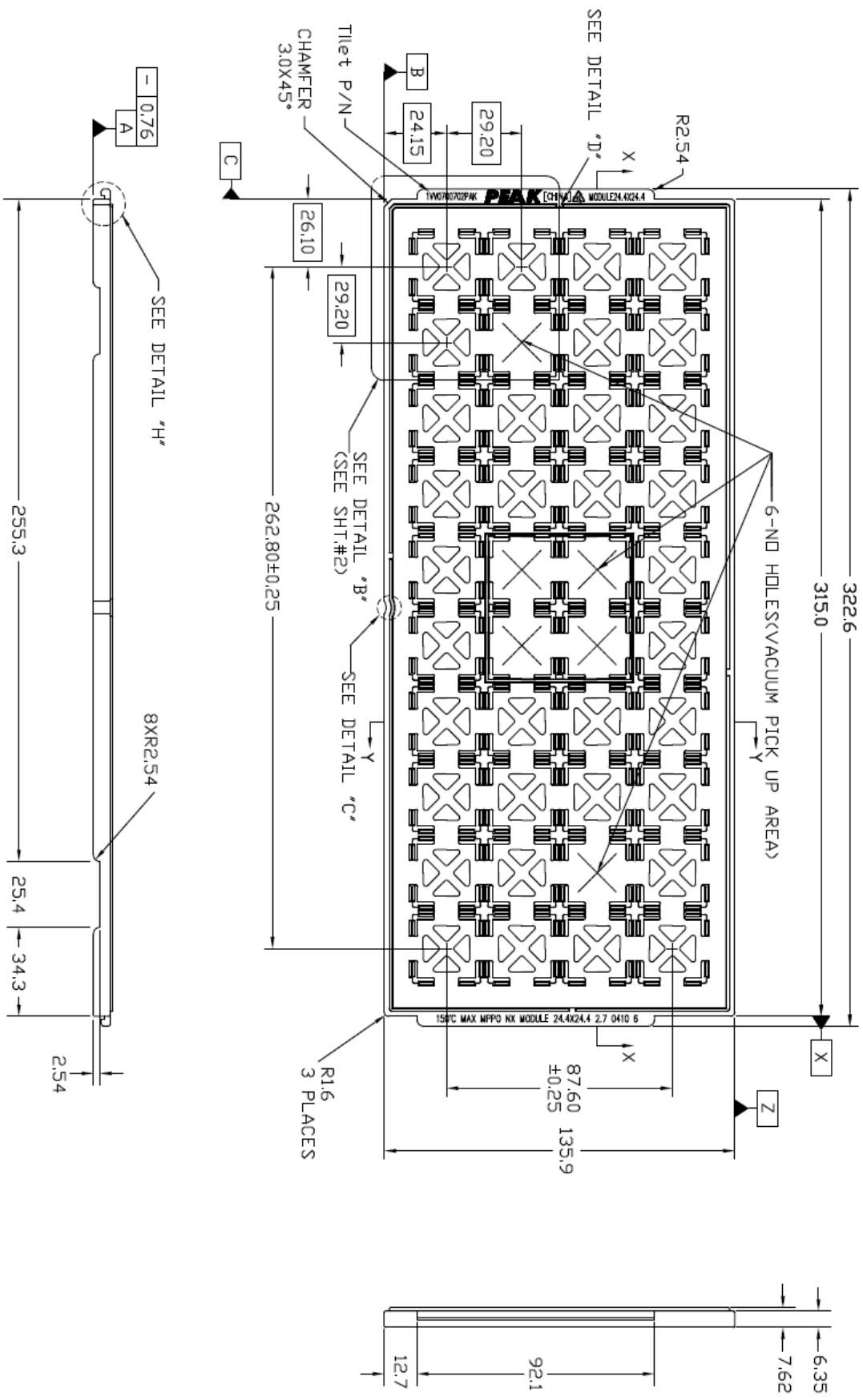
Is possible to order in two packaging system:

- Package on tray
- Package on reel

9.1. Tray

The NL865H2 modules are packaged on trays of 40 pieces each. These trays can be used in SMT processes for pick & place handling.

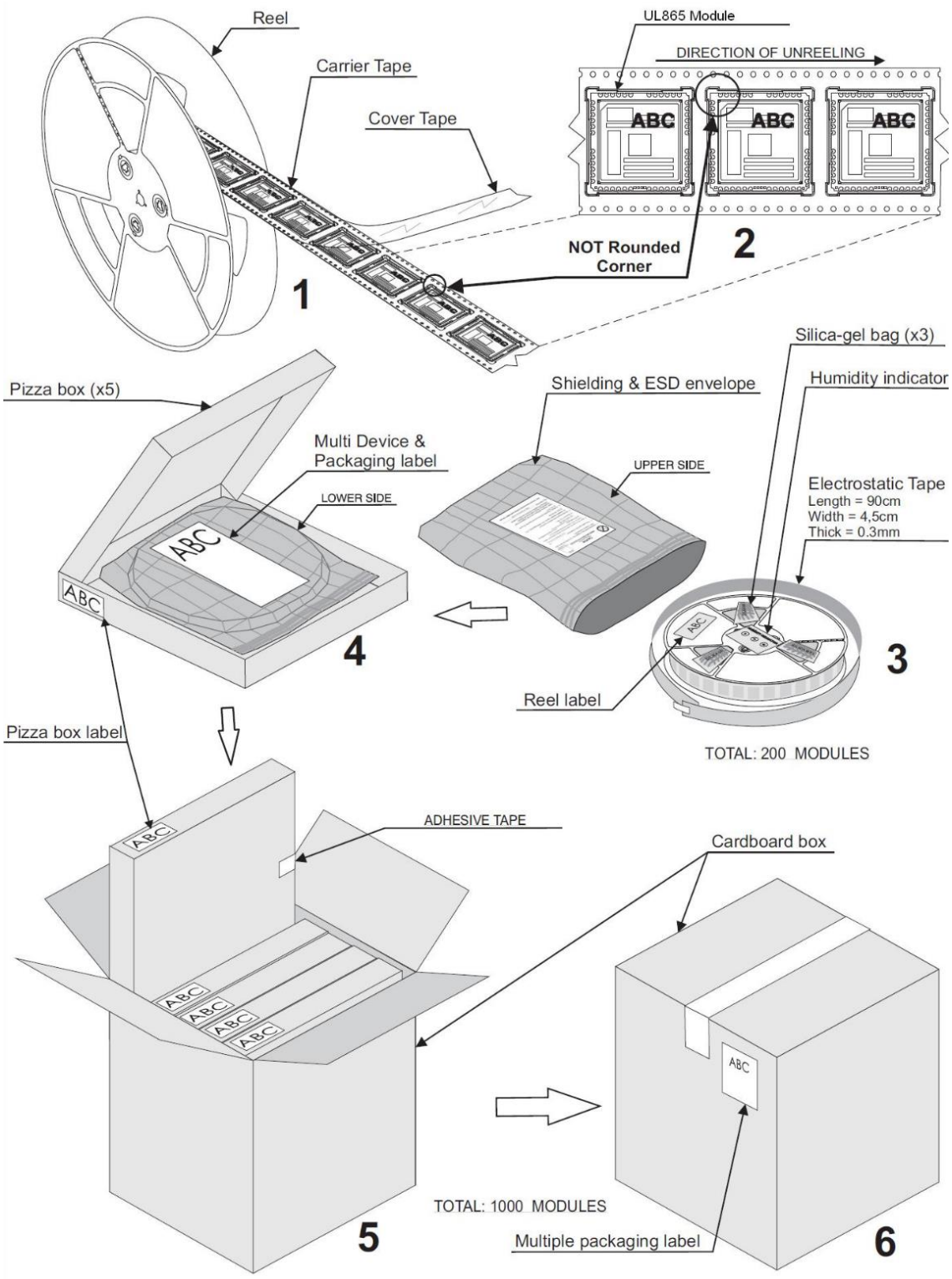



SEE DETAIL "D"
R2.54
CHAMFER 3.0X45°
Tilet P/N
B
24.15
29.20
C
26.10
29.20
SEE DETAIL "B" (SEE SHT.#2)
SEE DETAIL "C"
SEE DETAIL "H"
262.80±0.25
255.3
6-NO HOLES(VACUUM PICK UP AREA)
315.0
322.6
8XR2.54
25.4
34.3
2.54
R1.6
3 PLACES
87.60
±0.25
135.9
X
Y
Z
12.7
92.1
7.62
6.35

9.2. Reel

The NL865H2 can be packaged on reels of 200 pieces each.

See figure for module positioning into the carrier.



9.3. Moisture sensitivity

The moisture sensitivity level of the Product is “3” according with standard IPC/JEDEC J-STD-020, take care of all the relative requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) The shelf life of the Product inside of the dry bag is 12 months from the bag seal date, when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH.
b) Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033B paragraph 5.2” is respected.
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

10. SAFETY RECOMMENDATIONS

10.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available,

while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

11. CONFORMITY ASSESSMENT ISSUES

11.1. Approvals

- RED
- RoHS and REACH

11.2. Declaration of Conformity

The DoC is available here: https://www.telit.com/RED/

12. SAFETY RECOMMENDATIONS

12.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the LTE network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

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while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

13. REFERENCE TABLE OF RF BANDS CHARACTERISTICS

Band	Freq. Tx (MHz)	Freq. Rx (MHz)
B1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz
B2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz
B3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz
B4	1710 MHz – 1755 MHz	2110 MHz – 2155 MHz
B5	824 MHz – 849 MHz	869 MHz – 894 MHz
B8	880 MHz – 915 MHz	925 MHz – 960 MHz
B12	699 MHz – 716 MHz	729 MHz – 746 MHz
B13	777 MHz – 787 MHz	746 MHz – 756 MHz
B17	704 MHz – 716 MHz	734 MHz – 746 MHz
B18	815 MHz – 830 MHz	860 MHz -875 MHz
B19	830 MHz – 845 MHz	875 MHz – 890 MHz
B20	832 MHz – 862 MHz	791 MHz -821 MHz
B25	1850 MHz – 1915 MHz	1930 MHz -1995 MHz
B26	814 MHz – 849 MHz	859 MHz – 894 MHz
B28	703 MHz – 748 MHz	758 MHz – 803 MHz
B66	1710 MHz – 1780 MHz	2110 MHz – 2200 MHz
B71	663 MHz – 698 MHz	617 MHz – 783 MHz
B85	698 MHz – 716 MHz	728 MHz – 746 MHz

14. ACRONYMS

TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input

MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready
SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer
TTFF	Time to First Fix

15. DOCUMENT HISTORY

Revision	Date	Changes
0	2019-07-17	First emission – Preliminary
1	2019-08-20	Updated overall document
2	2019-09-30	Updated chapters 2.1, 4.1, 4.2, 6.1.1, 11.1
3	2019-10-10	Updated chapters 1.5, 2.2
4	2019-11-08	Watermark added
5	2020-03-18	Updated overall document
6	2020-04-01	Pinout table updated
7	2020-04-20	Updated chapters 4.1, 4.4.3

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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